

ALTERA® CYCLONE™ FPGA PROTOTYPE MODULE

# EzFPGA User Guide

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## Introduction

Thank you for purchasing Dallas Logic's EzFPGA evaluation module. This FPGA kit has everything you need to start designing with and evaluating the powerful features of Altera® Cyclone™ FPGA devices. The ezFPGA proto board allows you to add a powerful gate array to your prototype or home project easily and with minimal design overhead. The 1.7 x 3.0 inch module provides all FPGA support circuitry, so you can just plug and go with your own project. The kit provides an Altera Byte Blaster II FPGA programmer and a power supply. Individual ezFPGA modules (no kit components) are also available. Whether you just want to learn about FPGA design, or have a specific design implementation to complete, this evaluation module will jump-start the your own Cyclone™ efforts. Altera's Quartus II is a state of the art software tool which allows coding, compilation, and simulation of complex digital circuit designs in a programmable logic environment. Your EzFPGA kit includes the following items:

- EzFPGA evaluation module
- Wall mount type 5VDC/2A switching power supply (US or Asian/European model, depending on which was ordered)
- ByteBlaster II FPGA programmer
- Altera® “web-pack” Quartus II tools CD



Although the EzFPGA module will run by itself “out of the box”, you will need access to a PC to view and explore the reference design files. Altera's Quartus II software supports both Windows® and Linux operating systems. Consult Altera's website at [www.altera.com](http://www.altera.com) for specifics on operating system requirements. As of this writing, Quartus II version 3.0 for Windows® requires Microsoft Windows®

NT4.0 (SP3), 2000, or XP. Users who need support for Windows® 98 can download Quartus II Web Edition version 2.2 software including service pack 2. This version will support compilation of the Cyclone FPGAs.

A male to female DB25 “LPT printer port” cable will be required to connect Altera’s ByteBlaster II programmer cable to your PC (The ByteBlaster can be plugged directly into a notebook PCs LPT port, but the connector cable is only 11.5 inches long). See the section on Software and Hardware setup for more details on setting up your EzFPGA.

Note that Altera® and Cyclone™ are registered trademarks of Altera Corporation. Windows® is a registered trademark of Microsoft Corporation. No further reference to this will be made.

### **EzFPGA Module Quick Start**

To quickly see your EzFPGA module function, complete the following steps:

1. Locate your EzFPGA module and module so as to not short any of the pins on the bottom of the PCB. Make sure to clean away any loose wire or solder from the EzFPGA bench area.
2. Plug the external power-supply into a wall outlet. If outside the U.S., make sure you received the Asian/European model and have an appropriate plug adapter (supply input voltage is 230V AC, 50/60Hz in some areas overseas).
3. Connect the external power supply to J3 (1.3mm DC jack).
4. Your EzFPGA evaluation module will power-up and start driving the LED devices. All module pins are also sequentially toggled using a 20bit counter instantiated in the Quartus II logic design.

All pin headers are placed on 0.1 inch spacing to allow the use of standard prototyping “perf-module” with the EzFPGA.

**WARNING!!** Do not directly connect 5V devices to the ezFPGA IO pins. See the section on 5V interfacing for proper connection methods.



### Altera Cyclone Device

The EzFPGA evaluation module comes populated with one Altera EP1C3 Cyclone FPGA in the 144 pin TQFP package (U4). Modules come with the –8 device. The 144 pin EP1C3 device provides the following programmable logic resources:

- 104 user IO pins (95 available on EzFPGA module)
- 2910 Logic Elements ( approximately 50 gates per LE)
- 59,904 RAM bits or approximately 7.5K bytes (13 M4K RAM blocks which are 128x36 each)
- 1 PLL modules
- Four banks of user IO, each individually powered by separate VIO input pins.

Altera documents specify the following PLL operating frequencies based on speed grade:

Device	PLL Input Frequency	Maximum PLL output
EP1C3 -6	15.00-200 Mhz	312 Mhz
EP1C3 -7	15.00-181 Mhz	283 Mhz
EP1C3 -8	15.00-166 Mhz	260 Mhz

The maximum operating frequency of a logic design is dependent on the number/speed of logic delays and the logic fit/placement to the device. Consult Altera's [Cyclone Device Handbook](#) for more information on internal device timing and design speed estimation.

### EPCS1 serial flash

The EPCS1 serial flash device (U1) is used to load the FPGA hardware configuration data. The EPCS1 device is a 1Mbit device and contains 1,048,576 bits of program space. The EP1C3 FPGA requires 627,376 bits (non-compressed) for its configuration load, which leaves approximately 421,200 bits (52.6K bytes) for processor software images or user data.

The EPCS1 device supports byte or buffer moves of data, and also has software driver and interface support via Altera's SOPC builder.

## ByteBlaster II Programming Headers

Two separate 10 pin programming headers are provided on the EzFPGA module. One header is for the ASMI flash interface (J2) on the EPCS1/Cyclone devices, and the other is for the Cyclone JTAG port (J1). Two separate programming ports allows the EzFPGA design to support Flash reads and writes at the same time the JTAG port is being used for operations like Altera SignalTap logic analyzer (Quartus II feature), or in-circuit debug. The ASMI port is used to program the FPGA load into the EPCS1 flash device. Note that pins 1 of both the JTAG (J1) and ASMI (J2) connectors are located towards the “bottom” of the PCB assembly (silkscreen shows pin 1 and pin 10 on each connector). When plugging in the Byte Blaster II programmer, the red wire identifies pin 1 and the ribbon connector should be plugged in with the red wire towards the “bottom” (towards the 3 LED devices) on both J1 and J3.

## Reset Circuit

The EzFPGA module provides a TPS3802 voltage monitor (U6). The reset input (pin 3 of J2 which is FPGA conf\_done) of this device is active low and the device reset output drives the dedicated reset pin on the Cyclone FPGA device. A Quartus II setting defines this Cyclone FPGA pin to be either a dedicated chip wide reset or a user IO. Even if the pin is defined as user IO, the signal can still be used to reset individual circuits within a given design.

The TPS3802 will provide a 400mS reset pulse for the following events:

- Module power up
- Grounding of J2, pin 3 (open drain conf\_done signal)
- 3.3V power out of range
- Following FPGA configuration and loading

During FPGA initialization, the conf\_done (open drain) pin from the FPGA asserts the MR- (manual reset) input pin of the TPS3802 and causes a logic reset to the FPGA and any external devices connected to the reset signal on the pin header. Once the FPGA has finished loading, conf\_done will float high, and reset will de-assert approximately 400ms after FPGA configuration has finished.

## FPGA User IO Banks

There are four separate IO banks on the Cyclone device. Each has its own power pins so that multiple IO types can be supported from a single Cyclone device (IO Bank voltages in addition to the 1.5V core voltage). On the EzFPGA module, banks 1,2 and 3 are powered with 3.3V. Bank 4 is also powered with 3.3V, but through 0 ohm resistor R10. This allows lifting of the resistor and powering with a different IO voltage if desired. Pin headers are labeled on the PCB according to their associated IO bank number (J100-B3, J100-B4, J101-B1, J101-B2).

## Indicator LED

The EzFPGA module provides three general purpose LED outputs (green, yellow, red). Schematic page 7 shows the LED devices. B3 IO\_19, IO\_20, and IO\_21 are used to drive the LED devices. The Quartus II starter design connects these pins to the LEDs.

### Clock Oscillator

There is a 24.000 Mhz oscillator (U1) installed on your EzFPGA module. This value is evenly divisible by a baud rate of 19.2K ( $1250 \times 19200 = 24000000$ ). It also works well to generate max data rates, and is above the 15.0 Mhz required minimum PLL input frequency for Cyclone FPGAs.

EzFPGA Part Number	Device	PLL Input Frequency	Max. Specified PLL output	PLL Ratios at 24Mhz
EzFPGA-8	EP1C3 -8	15.00-166 Mhz	260 Mhz	$(24 * 4/3) * 8 = 256$

Altera EP1C3 devices support one on-chip PLL module. Other PLL ratios can be implemented depending on design clock requirements.

## Software and Hardware Setup

### EzFPGA Module Setup

Detailed steps to configure and run your EzFPGA module are:

1. Locate the PCB and module so as to not short any of the pins on the bottom of the PCB. Make sure to clean away any loose wire or solder from the EzFPGA bench area.
2. Connect the ByteBlaster II cable to J1 (JTAG) programming header.
3. Plug the external power-supply into a wall outlet. If outside the U.S., make sure you received the Asian/European model and have an appropriate plug adapter (supply input voltage is 230V AC, 50/60Hz in some areas overseas).
4. Connect the external power supply to J1 (1.3mm DC jack).

Note that the EzFPGA module can accept 4V-6V input voltage via the 1.3mm DC jack (J1-center pin positive). It can also be powered by using pin 1 and pin 2 of J101-B1 (for use with a bench-top power supply). Pin 1 is Input Ground and Pin 2 is for power voltage input. J101-B1 also provides power output pins which are pin 4 for VIO (3.3V), and pin 3 for VCORE (1.5V). These outputs can be used to power external components connected to the EzFPGA assembly. The input fusing on the EzFPGA module is limited to 1A. For bench-top power supply operation the EzFPGA is designed to operate at 4V-6V and requires approximately 50 mA of current. Do not exceed this voltage specification when applying external power.

### Altera Software and ByteBlaster II

Your EzFPGA comes with Altera's Web-pack development CD and a ByteBlaster II programming cable. The Web-pack CD should be installed on your PC to provide Quartus II and Nios/SOPC support (Nios/SOPC install is optional and requires a lot of disk space). Quartus II is used to compile your design files and Program the Cyclone FPGA on the EzFPGA module (via the ByteBlaster II programmer).

Nios/SOPC installation is required only to support implementation of Nios processor designs. Quartus II version 3.0 for Windows requires Microsoft Windows NT4.0 (SP3), 2000, or XP. Users who need support for Windows 98 can download Quartus II Web Edition version 2.2 software including service pack 2. You may be required to request a web-pack license from Altera, even though the software is essentially free.

Web-pack Quartus II provides incredible design capability and fully supports the Cyclone line of FPGA devices (web pack has limited compile functionality for Stratix and higher end FPGA devices). The web-pack SOPC builder version is a trial version and implements a “clock-counter” limitation for Nios processors. This means that a Nios processor instantiated with web-pack will quit functioning after a few days (dependent on clock frequency). For learning or testing on the EzFPGA module this is not a serious limitation, but to implement working Nios designs on your own products, you will have to acquire a full Nios license from Altera.

The ByteBlaster II cable is plugged into the LPT (printer) port of your Windows/Linux PC. For detailed information on Quartus II/ByteBlaster II installation, setup, and requirements access [www.altera.com](http://www.altera.com) and reference their online documentation.

## **5V and external Interfacing**

**WARNING!!** Do not directly connect 5V devices to the ezFPGA IO pins. Read further for proper 5V connection methods.

Cyclone FPGA devices provide interfacing capability for multiple IO standards, and flexibility in interfacing. By choosing the right VIO voltage, various IO standards can be supported. But, Cyclone devices do not support 5V VIO and therefore 5V interfacing techniques must be given special attention. From Altera’s Cyclone Device Handbook, section 11, the main interfacing features that Cyclone FPGA devices provide are:

- Hot-Socketing—add and remove Cyclone devices to and from a powered-up system without affecting the device or system operation
- Power-Up Sequence flexibility—Cyclone devices can accommodate any possible power-up sequence
- Power-On Reset—Cyclone devices maintain a reset state until voltage is within operating range

Please refer to chapter 11 of Altera’s Cyclone Device Handbook for details on Cyclone IO interfacing. Cyclone FPGA devices provide a separate IO and core voltage power structure.

The first main consideration for 5V operation is PCI clamping diodes on the Cyclone FPGA IO pins (which are enabled by the user, during re-configuration, or if the FPGA device is not configured). The PCI clamping diodes will cause 5V signals being driven to the FPGA to essentially be shorted to ground via a 4.1V clamping diode. In this situation series resistors are required to limit the current flow out of the 5V driving pin. The second main consideration is the V-high voltage of the Cyclone IO pin that is driving

to a 5V device. For TTL type 5V devices, the drive voltage is sufficient (voltage above 2.4V). For 5V CMOS type devices, the drive voltage may not be sufficient to signal a high voltage level to the 5V device. Note that adding a pull-up resistor will not provide a higher voltage than the output voltage that is being driven by the Cyclone IO pin.

Make sure you **properly configure any 5V circuits** which you attach to the EzFPGA module (add series resistors and check voltage high requirements). Improper connection of 5V circuits can **damage the EzFPGA Cyclone FPGA** or the external components which you are interfacing to. Finally, also make sure you do not exceed the power and current capability of the EzFPGA module when connecting and powering external devices using module power (EzFPGA power input has a 1 amp fuse at 4V-6V DC).

### **FPGA Reserved Pins – ezFPGA Design**

The ezFPGA PCB design provides for use of both the EP1C3 and EP1C6 FPGA devices. This requires that six of the IO pins on the EP1C3 be reserved for EP1C6 power connections (on the ezFPGA PCB). These EP1C3 IO pins are connected to the VCC and GND power planes and should only be configured as tri-state for EP1C3 FPGA designs which are created for the ezFPGA module. The Quartus II starter design has these pins reserved properly. These pins are: 54, 55, 91, 94, 126 and 127.

### **Altera Reference Documents**

This User Manual is a guide to the EzFPGA reference design as well as a “quick start” guide for basic Quartus II operations. It is not intended to replace the standard set of Altera documentation which is necessary for detailed design of Cyclone FPGA systems. All of Alteras documentation is available online at [www.altera.com](http://www.altera.com). In particular, the following documents should be referenced:

- Cyclone Device Handbook , Volume I and II  
[http://www.altera.com/literature/hb/cyc/cyclone\\_device\\_handbook.pdf](http://www.altera.com/literature/hb/cyc/cyclone_device_handbook.pdf)
- Serial Configuration Devices Datasheet,  
[http://www.altera.com/literature/hb/cyc/cyc\\_c51014.pdf](http://www.altera.com/literature/hb/cyc/cyc_c51014.pdf)
- Nios 32bit Programmers Reference Manual,  
[http://www.altera.com/literature/manual/mnl\\_nios\\_programmers32.pdf](http://www.altera.com/literature/manual/mnl_nios_programmers32.pdf)
- Nios Avalon Bus Specification and Reference Manual,  
[http://www.altera.com/literature/manual/mnl\\_avalon\\_bus.pdf](http://www.altera.com/literature/manual/mnl_avalon_bus.pdf)
- Nios UART Data Sheet,  
[http://www.altera.com/literature/ds/ds\\_nios\\_uart.pdf](http://www.altera.com/literature/ds/ds_nios_uart.pdf)
- Nios PIO Data Sheet,  
[http://www.altera.com/literature/ds/ds\\_nios\\_pio.pdf](http://www.altera.com/literature/ds/ds_nios_pio.pdf)

- Nios Timer Data Sheet,  
[http://www.altera.com/literature/ds/ds\\_nios\\_timer.pdf](http://www.altera.com/literature/ds/ds_nios_timer.pdf)
- GNUpro Users Guide,  
[http://www.altera.com/literature/third-party/nios\\_gnupro.pdf](http://www.altera.com/literature/third-party/nios_gnupro.pdf)
- Nios Embedded Processor Software Development Reference Manual  
[http://www.altera.com/literature/manual/mnl\\_niosft.pdf](http://www.altera.com/literature/manual/mnl_niosft.pdf)

## EzFPGA Quartus II Starter Design

Your EzFPGA module comes with the EzFPGA starter design stored in the EPCS1 flash device. After applying power to the module, the LED devices will illuminate, and the module pins will be toggled by the EzFPGA counter circuit. All of the FPGA IO pins are defined making it an easy job to connect the IO pins to your own logic circuits. To modify and add to the design, you will need to obtain the starter design project files and software source code. These files are available for download from the Dallas Logic website. These files should be copied to a project file in your PC's Altera Quartus II installation folder.

For the EzFPGA starter design, Altera “megafunction” blocks were instantiated for logic circuit functionality, and then graphical representations of those blocks (.bdf files) were “stitched” together using Altera’s graphical editor. This creates the top-level graphical “.bdf” design file (hierarchical design). Quartus II supports VHDL, Verilog, and AHDL (Altera HDL). Verilog and VHDL are more “mainstream” and both are standards in the design industry. AHDL is Altera’s own HDL syntax, and is very similar to ABEL. AHDL is very simple to use and is still very powerful. AHDL is a good language to learn for those who are just getting started in FPGA design and HDL. Verilog is the syntax that SOPC builder uses when generating design modules. You can use both the Altera megafunction blocks, or your own logic blocks that you code using an HDL. The graphical representations of these blocks can also be added to the top level design .bdf file.

### Quartus II Tutorial Instructions

After installation of your Quartus II web edition CD, it is highly recommended that you go through the exercises contained in the Quartus II tutorial. The tutorial will help you to become comfortable with the QII 3.0 development environment.

Launching QII:

- Double click the Quartus II shortcut (icon) found on the desktop of your computer.
- Allow the computer to search the Altera site for updates. This will ensure that you have the latest copy of web edition.
- Under the Help menu on the top toolbar, select tutorial.

- At the top of the tutorial window push the Next button this will take you through tutorial basics and into the design sections.

Once you have completed the tutorial sections you will be ready to explore the EzFPGA design.

The EzFPGA design can be found in the top.bdf file of the EzFPGA project directory. The EzFPGA designs top level module was created using Altera's schematic editor. The schematic allows the user to create graphical block representations for sub-modules. These sub-modules can then be stitched together using "wires" for connectivity.

### **EzFPGA Starter Design File Install**

The EzFPGA starter design files are located on the Dallas Logic website in the "Altera Eval Boards" section. Download the starter design .zip file to your machine and unzip the .qar file to an Altera project folder on your computer. Altera design archive files have the extension .qar, and contain all the necessary source files to rebuild the original project folder. You must boot Quartus II, and under the "Project" menu select the "Restore Archived Project" selection. You can then go into the restored project directory and open the "top.bdf" top level project file. This file shows the schematic representation of the EzFPGA starter design.

### **Reference Design Schematic**

The EzFPGA schematic should be referenced for details on circuit design or when connecting devices to the supplied pin-headers. The schematics .pdf pages are available for download from [www.dallaslogic.com](http://www.dallaslogic.com)

### **EzFPGA Module Technical Help**

Being an "internet-centric" company, Dallas Logic provides manned 24hr email and web forum support. The best way to obtain help with problems is to post questions to our online support forum. We are prompt about replying, and there is also a good chance you will find your question has already been answered online in the forum. If you prefer email support, we can be reached at [support@dallaslogic.com](mailto:support@dallaslogic.com). We will generally reply within 24hrs of receiving an inquiry or request for help with problems which are related to the operation of your EzFPGA module. Before contacting us with inquiries, please make sure you have:

1. Verified the fuse (F1) and checked the voltage outputs at connector J101-B1 (pin 3,4).
2. Removed any test circuits from connection to the EzFPGA PCB and restored it to its original design state (remove and restore any modifications).
3. Re-programmed and tested your EzFPGA module with the original reference design files.

For questions related specifically to Altera software tools or FPGA devices, we can sometimes be of assistance, but will generally refer you to the Altera online knowledge base or online support web pages.

**Warranty Information**

Your un-modified EzFPGA assembly is guaranteed to be free of defects in material and workmanship for a period of ninety days from the date of purchase. If your EzFPGA module stops working during the ninety day period, and is in its original, un-modified state, first contact us at [support@dallaslogic.com](mailto:support@dallaslogic.com). If the problem cannot be resolved, you must return the PCB assembly and power supply, postage prepaid to Dallas Logic Corporation. All repairs and return ship will be made within 12 days of receipt of package. During the warranty period, Dallas Logic will, at its option, repair, replace, or refund the purchase price. Products that have been damaged or modified from their original design state are not covered by warranty. No warranty is implied with respect to the software or firmware files.

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