ALTERA® CYCLONE II™ FPGA MODULE

Niomite User Guide

2300 McDermott #200-305
Plano, TX 75025
www.dallaslogic.com

Version 1.0- January 2007

This document is the property of, and is maintained by Dallas Logic Corporation. Please post any questions, corrections, or suggestions to the Niomite user forum located online at www.dallaslogic.com. Dallas Logic Corporation shall under no circumstances be liable for damages or related expenses resulting from the use of this document. Your use of this information indicates your understanding of, and agreement with the disclaimer located on the last page of this document.

Table of Revisions

Revision	Author	Date	Description
0.1	ET	05-12-06	Draft release of User Guide
1.0	ET	01-16-07	First release of User Guide

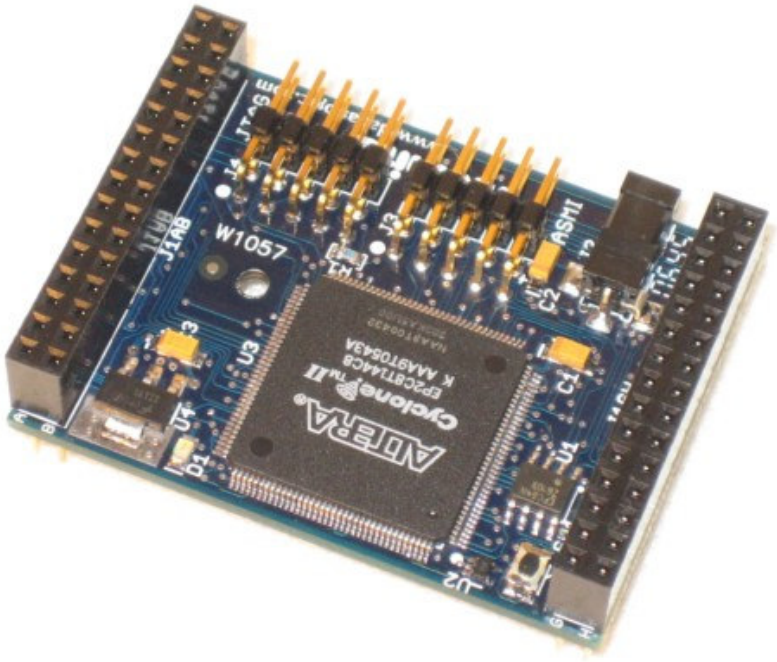
Table of Contents

Introduction

Thank you for purchasing Dallas Logic's Niomite FPGA module. The Niomite was designed to allow implementation of FPGA logic functions and/or Altera Nios II processor operation in the smallest possible form factor. The 1.6 x 2.1 inch module provides all FPGA support circuitry, so you can just plug and go with your own project. The Niomite module contains the following active devices:

- 512K X 8 SRAM
- EP1S4 FPGA serial loader (FPGA and Nios boot)
- 25 MHz oscillator
- Reset and voltage monitor

Niomite also supports the **cardstac** specification (master or slave half card), and can interface with other modules designed to that specification.

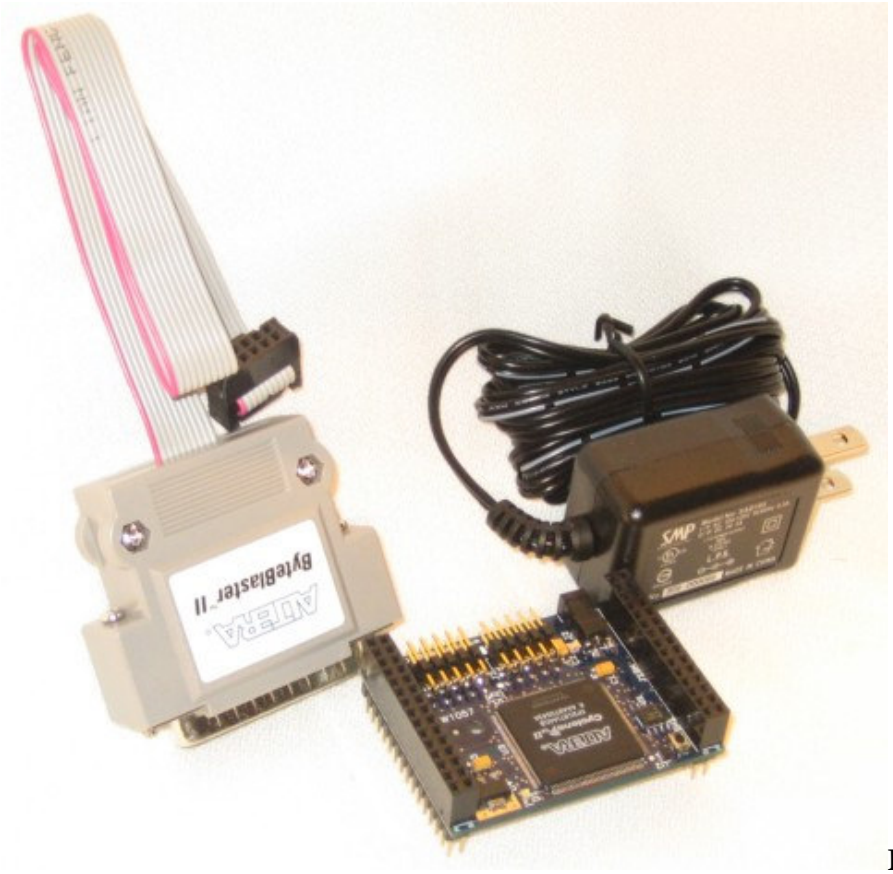


Niomite Module

The Niomite FPGA kit has everything you need to start designing with and evaluating the powerful features of Altera® Cyclone II™ FPGA devices. The kit provides an Altera Byte Blaster II or USB Blaster FPGA programmer and a power supply. Individual Niomite modules (no kit components) are also

available. Whether you just want to learn about FPGA design, or have a specific design implementation to complete, this evaluation module will jump-start the your own Cyclone II™ design efforts. Altera's Quartus II is a state of the art software tool that allows coding, compilation, and simulation of complex digital circuit designs in a programmable logic environment. Your Niomite kit includes the following items:

- Niomite module
- Wall mount type 3.3VDC/2A switching power supply (Asian/European plug option, depending on geographic location)
- Altera® ByteBlaster II or USB Blaster FPGA programmer



Byte Blaster Kit

USB Blaster Kit

Altera Quartus II web edition software must be downloaded from Altera's website. Although the Niomite module will run by itself "out of the box", you will need access to a PC to view and explore the reference design files. The starter design that is pre-programmed on the Niomite module does not include a Nios II processor instantiation. A reference design file for the Niomite that includes a Nios II processor can be downloaded from www.dallaslogic.com. This Nios II project was written for Quartus II version 6.0 SP1, and may require some end user modification to support versions of Quartus II later than 6.0 SP1.

Altera's Quartus II software supports both Windows® and Linux operating systems, although the free "web edition" only supports Windows 2000™ or Windows XP™. Consult Altera's website at www.altera.com for specifics on operating system requirements.

A male to female DB25 "LPT printer port" cable will be required to connect Altera's ByteBlaster II programmer cable to your PC (The ByteBlaster can be plugged directly into a notebook PCs LPT port, but the connector cable is only 11.5 inches long). If an Altera "USB Blaster" is utilized, then a free USB port is required on your PC.

Note that Altera® and Cyclone II™ are registered trademarks of Altera Corporation. Windows® is a registered trademark of Microsoft Corporation.

Niomite Module Quick Start

To quickly see your Niomite module function, complete the following steps:

1. Locate your Niomite module so as to not short any of the pins on the bottom of the PCB. Make sure to clean away any loose wire or solder from the Niomite bench area.

2. Plug the external power-supply into a wall outlet. If outside the U.S., make sure you received the Asian/European model, and have the appropriate plug adapter (supply input voltage is 230V AC, 50/60Hz in some areas overseas).

3. Connect the external power supply to J2 (0.65 mm DC jack). If a power supply was not ordered, then connect 3.3V to header pin J1-H1 and GND to header pin J1-H2.

4. Your Niomite evaluation module will power-up and start flashing the green LED device D1. All module pins are also sequentially toggled using a counter instantiated in the Quartus II logic design.

All pin headers are placed on 0.1 inch spacing to allow the use of standard prototyping "perf-board" with the Niomite.

WARNING!! Do not directly connect 5V devices to the Niomite IO pins. See the section on 5V interfacing for proper connection methods.

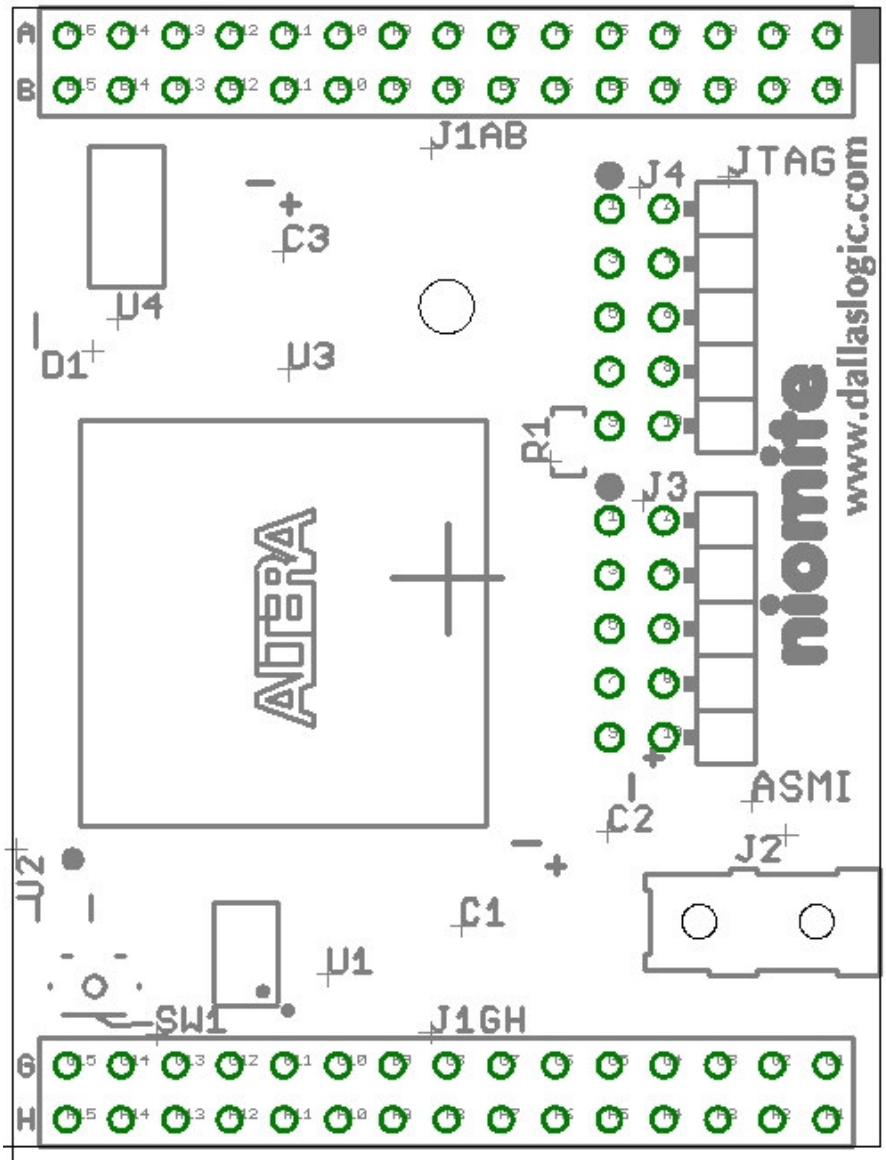
Component Descriptions

Specific components of the Niomite module design are:

- Altera EP2C5 or EP2C8 Cyclone II FPGA, in the –C8 speed grade.
- Separate programming ports (ASMI flash interface and JTAG interface).
- Reset and voltage monitor IC which provides 400mS reset pulse.
- Reset push-button switch.
- 44 input/output and 7 input pins available.
- 1 discrete indicator LED (green).
- Clock oscillator (25 MHz).
- cardstac compatible design.

- EPCS4 (4Mbit) serial flash for FPGA configuration and non-volatile storage (Nios II software image and data).
- 512K x 8 bit (4Mbit) SRAM for Nios II program execution and data storage.

Shown below is a silkscreen image of the Niomite PCB. You can use this image to help locate device reference designators or pin numbers on the header connectors.



Altera Cyclone II Device Resources and Performance

The Niomite module can be ordered with an Altera EP2C5 or EP2C8 Cyclone II FPGA in the 144 pin TQFP package (U3). Modules come with the –C8 speed grade device. The 144 pin devices provides the following programmable logic resources:

Device	T144 Package IO Pins	Niomite IO Pins	Logic Elements	PLL Devices/Global clock nets	M4K devices/RAM bits
EP2C5T144	89	44 IO 7 Input	4608	2 / 8	26 / 119808
EP2C8T144	85	44 IO 7 Input	8256	2 / 8	36 / 165888

Altera documents specify the following PLL and circuit operating frequencies:

Device	Minimum PLL Input Frequency	Maximum PLL output (to global clock net)	16 bit Counter (Max)	M4K Memory (Max)	1857 LE FFT Function (Max)
EP2C5-C8 EP2C8-C8	10 MHz	402.5 MHz	310 MHz	163 MHZ	96 MHz
EP2C5-C7 EP2C8-C7	10 MHz	402.5 MHz	349 MHz	195 MHz	119 MHz
EP2C5-C6 EP2C8-C6	10 MHz	402.5 MHz	401 MHz	235 MHz	141 MHz

Even though the PLL components are specified equally in all device speed grades, maximum logic circuit speed does vary with selected device speed grade. Some useful performance benchmarks can be found on pages 5-15, 5-16 and 5-17 of the Cyclone II specification. The maximum operating frequency of a logic design is dependent on the number of logic levels and the specific logic fit/placement of the design to the device. Consult Altera's Cyclone II Device Handbook for detailed information on internal device timing and design speed estimation.

Some benchmark numbers for Altera's Nios II processor are also shown in the table below. These numbers are taken directly from Altera's "Nios II Performance Benchmarks" document (not from Niomite design benchmarks). The Niomite design uses four bus cycles to fetch a single instruction from the external 8 bit memory device. The DMIPS values shown below are for single cycle memory access (not possible on Niomite). Utilization of a sizable on-chip cache will improve Niomite Nios processor performance. Finally, note that the LE utilization for the Nios II does not include items such as a UART or timer. Both of these devices require approximately 150 LE each.

Device	Maximum Frequency Nios IIe	Maximum Frequency Nios IIf	LE utilization Nios IIe	LE utilization Nios IIf
EP2C5-C8 EP2C8-C8			542	1595
EP2C5-C7 EP2C8-C7			542	1595
EP2C5-C6 EP2C8-C6	159 MHz/22 DMIPS at 0 wait state	126 MHz / 105 DMIPS at 0 wait state	542	1595

EPCS4 serial flash

The EPCS4 serial flash device (U4) is used to load the FPGA hardware configuration data. The EPCS4 device is a 4 Mbit device and contains 4,194,304 bits of program space. The EP2C5 FPGA requires 1,265,792 bits (non-compressed) for its configuration load, which leaves 2,928,512 bits (366K bytes) for processor software images or user data. The EP2C8 FPGA requires 1,983,536 bits (non-compressed) for its configuration load, which leaves 2,210,768 bits (276.3K bytes) for user data. Cyclone II devices support compression of FPGA configuration loads. Compression will typically provide 35% - 50% reduction in space requirements of the configuration load. This can be implemented if more user data space is required. Note that the size of the compressed FPGA load is not fixed, and will vary from compile to compile. The EPCS4 device supports byte or buffer moves of data, and also has software driver and interface support via Altera's SOPC builder.

512K X 8 SRAM

The 512K X 8 SRAM device (U101) is located on the bottom of the PCB. This device is primarily provided for Nios II or other CPU program and data storage. For Nios II processors (32 bit instruction), four SRAM access are required to fetch a single instruction. This is automatically handled by Nios dynamic bus sizing. The device is a Cypress CY7C1049CV33-15ZC (or equivalent), which is an asynchronous SRAM with an access time of 15 ns. On the Niomite design, the SRAM has a dedicated address/data bus to the FPGA device and does not share external header pins.

JTAG and ASMI Programming Headers

Two separate 10 pin programming headers are provided on the Niomite module. One header is for the ASMI flash interface (J3) on the EPCS4/Cyclone II devices, and the other is for the Cyclone II JTAG port (J4). Two separate programming ports allows the Niomite design to support Flash reads and writes at the same time the JTAG port is being used for operations like Altera SignalTap logic analyzer (Quartus II feature), or in-circuit debug. The ASMI port is used to program the FPGA flash image (.pof file) into the EPCS4 flash device. The JTAG port is used to program the SRAM image directly into the FPGA (.sof file). Note that pins 1 of both the JTAG (J4) and ASMI (J3) connectors are located towards the "top" of the PCB assembly (silkscreen dot indicates pin 1 on each connector). When plugging in the Byte Blaster II or USB Blaster programmer, the red wire identifies pin 1 and the ribbon connector should be plugged in with the red wire towards the "top" (towards the silkscreen dot) on both J3 and J4. See section "Niomite FPGA Programming Instructions" for more details on ASMI and JTAG programming procedures.

Reset Circuit

The Niomite module provides a TPS3802 voltage monitor (U2). The reset input (pin 3 of J3 which is FPGA conf_done) of this device is active low and the device reset output drives the dedicated reset pin on the Cyclone II FPGA device. A Quartus II setting defines this Cyclone II FPGA pin to be either a dedicated chip wide reset or a user IO. Even if the pin is defined as user IO, the signal can still be used to reset individual circuits within a given design.

The TPS3802 will provide a 400mS reset pulse for the following events:

- Module power up
- Grounding of J3, pin 3 (open drain conf_done signal)
- Press of SW1 push-button
- 3.3V power out of range
- Following FPGA configuration and loading

During FPGA initialization, the conf_done (open drain) pin from the FPGA asserts the MR- (manual reset) input pin of the TPS3802 and causes a logic reset to the FPGA. Once the FPGA has finished loading, conf_done will float high, and reset will de-assert approximately 400ms after FPGA configuration has finished. Note that this reset signal is driven locally to the FPGA only and is not connected to the PCB pin header. The FPGA must drive reset on the external pin utilizing your design parameters.

FPGA User IO Bank Voltage

There are four separate IO banks on the EP2C5 and EP2C8 Cyclone II devices. On the Niomite module, these four banks (1, 2, 3, and 4) are powered by 3.3V.

Indicator LED

The Niomite module provides one general purpose LED output (green). Schematic page 4 shows the LED device. The LED is connected to FPGA pin number 118, and header pin B12. The Quartus II starter design connects the LED to FPGA pin number 118. The LED can be illuminated by the FPGA or an external device that drives header pin B12. When pin B12 is to be used for IO only, the LED circuit can be disabled by removing the current limiting resistor (R107) from the PCB.

Software and Hardware Setup

Niomite Module Setup

Steps to setup and run your Niomite module are:

1. Locate the PCB and module so as to not short any of the pins on the bottom of the PCB. Make sure to clean away any loose wire or solder from the Niomite bench area.

2. Connect the ByteBlaster II or USB Blaster cable to J4 (JTAG) programming header.

3. Plug the external power-supply into a wall outlet. If outside the U.S., make sure you received the Asian/European model and have an appropriate plug adapter (supply input voltage is 230V AC, 50/60Hz in some areas overseas).

4. Connect the external 3.3V power supply to J2 (0.65mm DC jack). If a power supply was not ordered, then connect 3.3V to header pin J1-H1 and GND to header pin J1-H2.

The Niomite module will run and start to flash green LED D1.

Note that the Niomite module can accept 3.3V input voltage via the 0.65mm DC jack (J2-center pin positive). It can also be powered by using pin H1 and pin H2 of J1. Pin H2 is a ground pin, and pin H1 is a 3.3V power pin. J1-H1 can be used to input power to the Niomite, or if the DC JACK is attached to the Niomite, then pin H1 can provide power to external circuits. Do not connect the DC JACK to the Niomite if you have 3.3V attached to pin H1 from another power source. The current limit for pin H1 is 1 Amp, and this pin is fused with a 1.5A fuse. The Niomite 3.3V power rail is designed to operate at **3.14 – 3.46 V** (3.3V +/-5%).

Altera Software and FPGA Programmer

Your Niomite kit comes with a FPGA programming cable. The Quartus II Web edition software should be downloaded and installed on your PC to provide FPGA compilation and Nios II/SOPC support (Nios II/SOPC install is optional and requires extra disk space). Quartus II is used to compile your design files and Program the Cyclone II FPGA on the Niomite module (via the FPGA programmer cable). Nios II/SOPC installation is required only to support implementation of Nios II processor designs. Quartus II 6.0 web edition for Windows requires Microsoft Windows 2000 or XP. You will be required to request a

web edition license from Altera, even though the software is free of charge. Linux versions of Quartus II 6.0 require a full (paid) license.

Web edition Quartus II provides incredible design capability and fully supports the Cyclone II line of FPGA devices (web edition has limited compile functionality for Stratix and higher end FPGA devices). The web edition of Nios II/SOPC builder is a trial version and implements a "tether" limitation for Nios II processors. This means that a Nios II processor instantiated with trial software will quit functioning if disconnected from the Altera programmer. For learning or testing on the Niomite module this is not a serious limitation, but to implement working Nios II designs for your own products, you will have to acquire a full Nios license.

The ByteBlaster II cable is connected to the LPT (printer) port of your Windows/Linux PC. The USB Blaster is connected to a USB port. For detailed information on Quartus II/Blaster installation, setup, and requirements access www.altera.com and reference their online documentation.

Niomite FPGA Programming Instructions

The Niomite FPGA device can be programmed at any time using the JTAG port (using a .sof file), or by the EPCS4 serial flash device at board power up. A non-volatile flash image is loaded into the EPCS4 device (using a .pof file) by the user via the ASMI port. The two possible methods for programming the Niomite FPGA device are:

1. Use a .sof file and program the FPGA directly. To do this, connect the Byte-blaster to the JTAG port. Open the Altera programmer software and be sure "JTAG" Mode is selected. Next, click the "Auto Detect" button. Right click on the FPGA device that is listed and select "Change file". This will allow you to select a .sof file and assign it to the listed device. Finally, click the "Start" button to program the FPGA device. This is a temporary load. If power is removed the FPGA must be re-programmed.

2. Use a .pof file and permanently flash a new load into the EPCS4 device via the ASMI interface. To do this, attach the Byte-blaster to the ASMI port. Open the Altera programmer software and change to "Active Serial Programming" Mode. Select "Add file" and browse to your project .pof file. Finally, make the desired programming selections (check mark) and press the "Start" button. This will store the FPGA load in the serial flash device. Cycle power on the Niomite board to load the flash image into the FPGA device. Note that you cannot "auto-detect" on the ASMI port. **Important:** when the project file was compiled, you must have selected the EPCS4 as the target device and the mode as "Active Serial Programming". Other selections such as "Generate compressed bit-streams" must also be assigned at this time. These selections are found under the "Assignments – Device" menus in Quartus II (click the "Device and Pin Options" button and select the "Configuration" tab).

5V Interfacing With Cyclone II

WARNING!! Do not directly connect 5V devices to the Niomite IO pins. Read further for proper 5V connection methods.

Cyclone II FPGAs provide a separate IO and device core power structure. This flexible power structure supports multiple IO interface standards and "hot-socketing". On the Niomite module, the four FPGA IO power rails are tied to 3.3V. The main interfacing features that Cyclone II FPGAs devices provide are:

- Hot-Socketing—add and remove Cyclone II devices to and from a powered-up system without affecting the device or system operation
- Power-Up Sequence flexibility—Cyclone II devices can accommodate any possible power-up sequence
- Power-On Reset—Cyclone II devices maintain a reset state until voltage is within operating range

Cyclone II devices do not directly support 5V VIO and therefore special 5V interfacing techniques must be utilized. A major consideration for 5V IO pin operation are the voltage clamping diodes on the Cyclone II FPGA IO pins. These clamping diodes will cause 5V signals being driven to the FPGA to essentially be shorted to 3.3V via a clamping diode (resulting in the IO pin being held at approximately 4.1V). In this situation series resistors are required to limit the current flow out of the external 5V driving pin into the FPGA device pin. Another consideration is the V-high voltage of the Cyclone II IO pin that is driving to an external 5V level pin. For TTL type 5V devices, the drive voltage is sufficient (voltage above 2.4V). For 5V CMOS type devices, the drive voltage may not be sufficient to signal a high voltage level to the 5V device. Note that adding a pull-up resistor will not provide a higher voltage than the output voltage that is being driven by the Cyclone II IO pin. A level translator IC may be required for this case.

Make sure you **properly configure any 5V circuits** that are connected to the Niomite module (add series resistors and check voltage high requirements). Improper connection of 5V circuits can **damage the Niomite Cyclone II FPGA** or the external components that you are connecting to.

Niomite Module Power

Niomite 3.3V power pin H1 is specified at **1 Amp**, and is protected by a 1.5 Amp fuse. The 3.3V power rail should operate in the range of 3.14V - 3.46V (3.3V +/-5%). Pin H1 is protected with fuse F101, and the 3.3V DC jack input J2 is protected with fuse F100. The Niomite power supply (DC jack) can be used to supply 3.3V power to circuits external to the Niomite module (via pin H1). If the opposite scenario is implemented, and power is to be supplied to the Niomite module via the header pin H1 (3.3V), do not plug the external power supply into the DC jack (power applied by both pin H1 and the DC jack). Make sure you do not exceed the current capability of the Niomite module when connecting and powering external devices.

FPGA Reserved Pins – Niomite Design

The Niomite PCB design provides for use of both the EP2C5 and EP2C8 FPGA devices. This requires that four of the IO pins on the EP2C5 device be reserved for EP2C8 power connections (on the Niomite PCB). These EP2C5 IO pins are connected to the VCCINT and GND power planes and should only be configured as tri-state for EP2C5 FPGA designs that are created for the Niomite module. The Quartus II starter design has these pins reserved properly. These EP2C5 device pins are: 26, 27, 80 and 81.

Input Only Header Pins – Niomite Design

J1 Header pins A11, A12, A14, A15, B13, B14, B15 are input only on the Niomite design. Due to resource limitations with the 144 pin Cyclone II FPGA package, these particular pins do not support an output function.

Cardstac Support – Niomite Design

The Niomite was designed to support the Cardstac specification. The following header pins have 1.8K Ohm pull-up resistors attached:

Pin H3 (RST-), R100

Pin A2 (1I2C_SCL), R111

Pin A3 (1I2C_SDA), R113

Pin A5 (IRQ4B-), R114

These resistors can be removed if pull-ups are not required for your particular design. Header pin B12 is also used to drive a green LED. To disable the LED, remove resistor R107. For more information on Cardstac, download the specification located at www.dallaslogic.com.

Altera Reference Documents

This User Manual is a guide to Niomite operation as well as a "quick start" guide for Quartus II operations. It is not intended to replace the standard set of Altera documentation that is necessary for detailed design of Cyclone II FPGA systems. All of Altera's documentation is available online at www.altera.com.

Niomite Quartus II Starter Design

Your Niomite module comes with the Niomite starter design stored in the EPCS4 flash device. After applying power to the module, the LED devices will illuminate, and the module IO pins will be toggled by a Niomite counter circuit. All of the FPGA IO pins are defined making it an easy job to connect nets of your own logic circuits to external pins. To modify and add to the design, you will need to obtain the starter design Quartus II project archive (.qar file). This file is available for download from the Dallas Logic website. This file should be "de-archived" to a project folder located on your PC.

For the Niomite starter design, Altera "mega-function" blocks were instantiated for logic circuit functionality, and then graphical representations of those blocks (.bdf files) were connected together using Altera's graphic schematic editor. This creates the top-level graphical ".bdf" design file (hierarchical design) from which, it is very easy to analyze and interpret design intent. Quartus II supports VHDL, Verilog, and AHDL (Altera HDL). Verilog and VHDL are more "mainstream" and both are standards in the design industry. AHDL is Altera's own HDL syntax, and is very similar to ABEL. AHDL is very simple to use and is still very powerful. Verilog is the syntax that SOPC builder uses when generating Nios II design modules. You can use both the Altera megafunction blocks, or your own logic blocks that you code using an HDL. The graphical representations of these HDL blocks can also be added to the top-level design file.

Niomite Starter Design File Install

The Niomite starter design files are located on the Dallas Logic website on the Niomite product page. Download the starter design .zip file to your machine and unzip the .qar file to an Altera project folder on your computer. Altera design archive files have the extension .qar, and contain all the necessary source files to rebuild the original project folder. You must boot Quartus II, and under the "Project" menu select the "Restore Archived Project" selection. You can then go into the restored project directory and open the ".qpf" project file. This file is the project file that contains the top-level block, and shows the schematic representation of the Niomite starter design. The starter design that is pre-programmed on the Niomite module does not include a Nios II processor instantiation. A reference design file for the Niomite that includes a Nios II processor can be downloaded from www.dallaslogic.com. This Nios II file was written for Quartus II version 6.0, and may require some end user modification to support later versions of Quartus II.

Quartus II Tutorial Instructions

After installation of your Quartus II web edition download, it is highly recommended that you go through the exercises contained in the Quartus II tutorial. The tutorial will help you to become comfortable with the QII 6.0 development environment.

Launching QII:

- Double click the Quartus II shortcut (icon) found on the desktop of your computer (or navigate to the Altera folder and double click the Quartus II program icon).
- Allow the computer to search the Altera site for updates. This will ensure that you have the latest copy of web edition.
- Under the Help menu on the top toolbar, select tutorial.
- At the top of the tutorial window push the Next button this will take you through tutorial basics and into the design sections.

Once you have completed the tutorial sections you will be ready to explore the Niomite design.

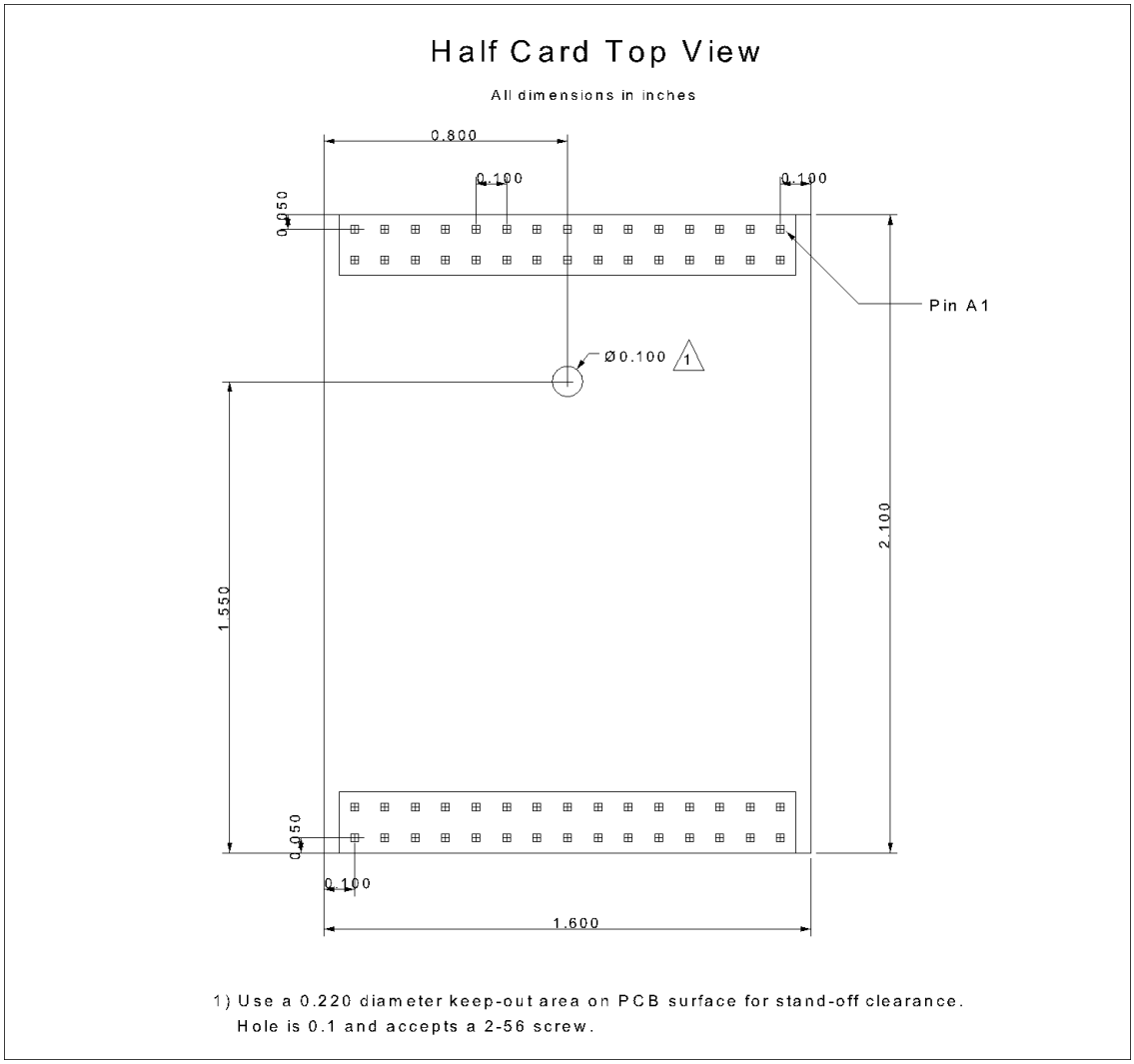
The Niomite design project can be opened from the ".qpf" file located in the Niomite project directory. The Niomite design top-level module (top.bdf) was created using Altera's schematic editor. The schematic allows the user to create graphical block representations for sub-modules. These sub-modules can then be stitched together using "wires" for connectivity.

Reference Design Schematic

Niomite schematic pages should be referenced for details on circuit design or when connecting devices to the supplied pin-headers. The schematic (.pdf file) pages are available for download from www.dallaslogic.com

Mechanical Dimensions

The mechanical dimensions for the Niomite module are shown in the diagram below.



Ordering and Technical Help

Niomite Ordering Information

Niomite and related products can be ordered directly from our website at www.dallaslogic.com. Orders can be shipped to almost any destination in the world. Shipping costs for orders can be obtained on the website before the order is finalized (submitted). Niomite part numbers are shown in the table below:

Part Number	Altera FPGA/Loader Device	Description
NIO-H-2C5-8	EP2C5T144C8/EPCS4SI8	Individual module (Cardstac half card configuration).
NIO-H-2C8-8	EP2C8T144C8/EPCS4SI8	Individual module (Cardstac half card configuration).
NIO-H-2C5-8-KB	EP2C5T144C8/EPCS4SI8	Kit including FPGA module, LPT port "Byte Blaster" programmer, and power supply.
NIO-H-2C8-8-KB	EP2C8T144C8/EPCS4SI8	Kit including FPGA module, LPT port "Byte Blaster" programmer, and power supply.
NIO-H-2C5-8-KU	EP2C5T144C8/EPCS4SI8	Kit including FPGA module, USB port "USB Blaster" programmer, and power supply.
NIO-H-2C8-8-KU	EP2C8T144C8/EPCS4SI8	Kit including FPGA module, USB port "USB Blaster" programmer, and power supply.

Niomite Module Technical Help

Being an "internet-centric" company, Dallas Logic provides manned 24hr email and web forum support. The best way to obtain help with problems is to post questions to our online support forum. We are prompt about replying, and there is also a good chance you will find your question has already been answered online in the forum. If you prefer email support, we can be reached at support@dallaslogic.com. We will generally reply within 24hrs of receiving an inquiry or request for help with problems that are related to the operation of your Niomite module. Before contacting us with inquiries, please make sure you have:

1. Verified fuses (F100 and F101 located on the bottom side of the PCB) and checked the 3.3V input level at header J1-H1.

2. Removed any test circuits from connection to the Niomite PCB and restored it to its original design state (remove any modifications and restore original circuits).

3. Re-programmed and tested your Niomite module with the original reference design files.

For questions related specifically to Altera software tools or FPGA devices, we can sometimes be of assistance, but will generally refer you to the Altera online knowledge base or online support web pages.

Warranty Information

Your un-modified Niomite assembly is guaranteed to be free of defects in material and workmanship for a period of ninety days from the date of purchase. If your Niomite module stops working during the ninety day period, and is in its original, un-modified state, first contact us at support@dallaslogic.com. If the problem cannot be resolved, you must return the PCB assembly and power supply, postage prepaid to Dallas Logic Corporation. All repairs and return ship will be made within 10 days of receipt of package. During the warranty period, Dallas Logic will, at its option, repair, replace, or refund the purchase price. Products that have been damaged or modified from their original design state are not covered by warranty. No warranty is implied with respect to the software or firmware files.

Disclaimer

Information in this document concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. Customers are advised to obtain the latest version of device specifications before relying on any published information. Dallas Logic Corporation DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DATA FILES, DEVICES, OR TECHNOLOGY described in this document. Dallas Logic Corp. also does not assume liability for intellectual property infringement related in any manner to use of information, devices, or technology described herein or otherwise. Dallas Logic Corp. makes no warranty of merchantability or fitness for any purpose and does not assume liability for damages incurred to property due to the use of this product or implementation of information or procedures listed in this document. Use of information or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.