ALTERA® MAX V CPLD MODULE

CMC5001 Quick Start Guide

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Table of Revisions

Revision	Author	Date	Description
1.0		04-28-2012	Release 1.0 of CMC5001 Quick Start Guide

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1. Introduction

Thank you for purchasing Dallas Logic's CMC5001 Cardstac module. The CMC5001 features Altera's MAX V 5M2210ZF324C5N. The CMC5001 module supports the cardstac specification (master or slave standard card, dual row 64 pin), and can interface with other modules designed to that specification. The module provides the following major features:

- 5M2210ZF324C5N MAX V with selectable I/O bank voltage
- Over 150 I/O pins available through the cardstac headers
- Three 25AA1024 1Mbit EEPROM
- TC77 Temperature sensor
- CARDSTAC Full card module with dual row footprint

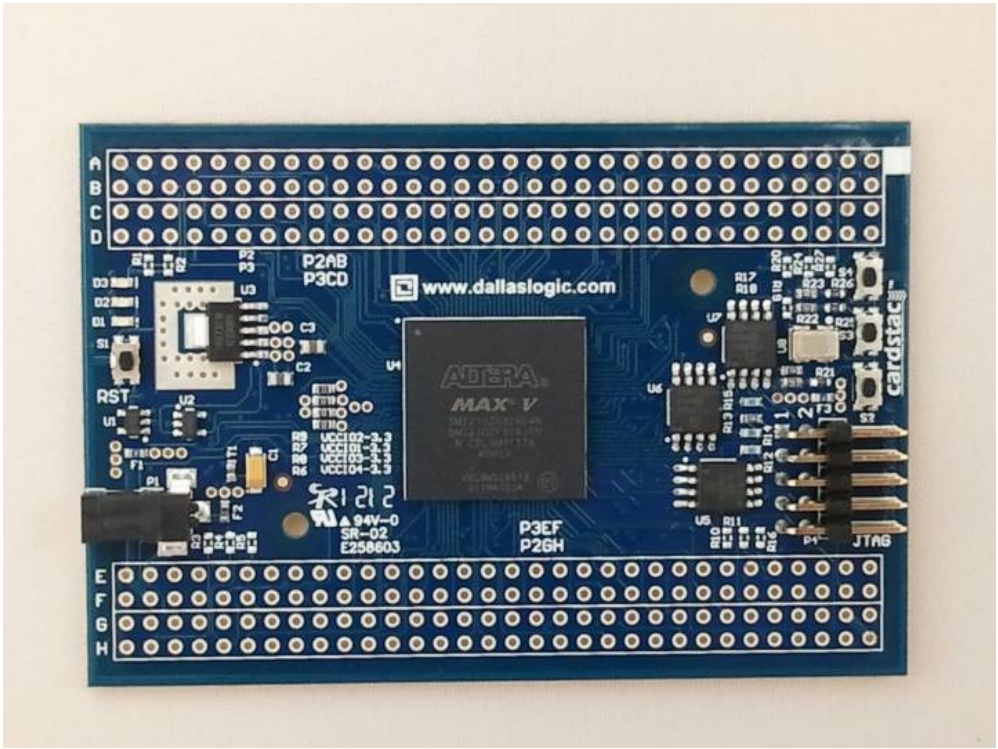

Figure 1-1 CMC5001 (5M2210ZF324C5N) Module

2. Component Identification

Shown below is a silkscreen image of the CMC5001 PCB. You can use this image to help locate device reference designators or pin numbers on the header connectors.

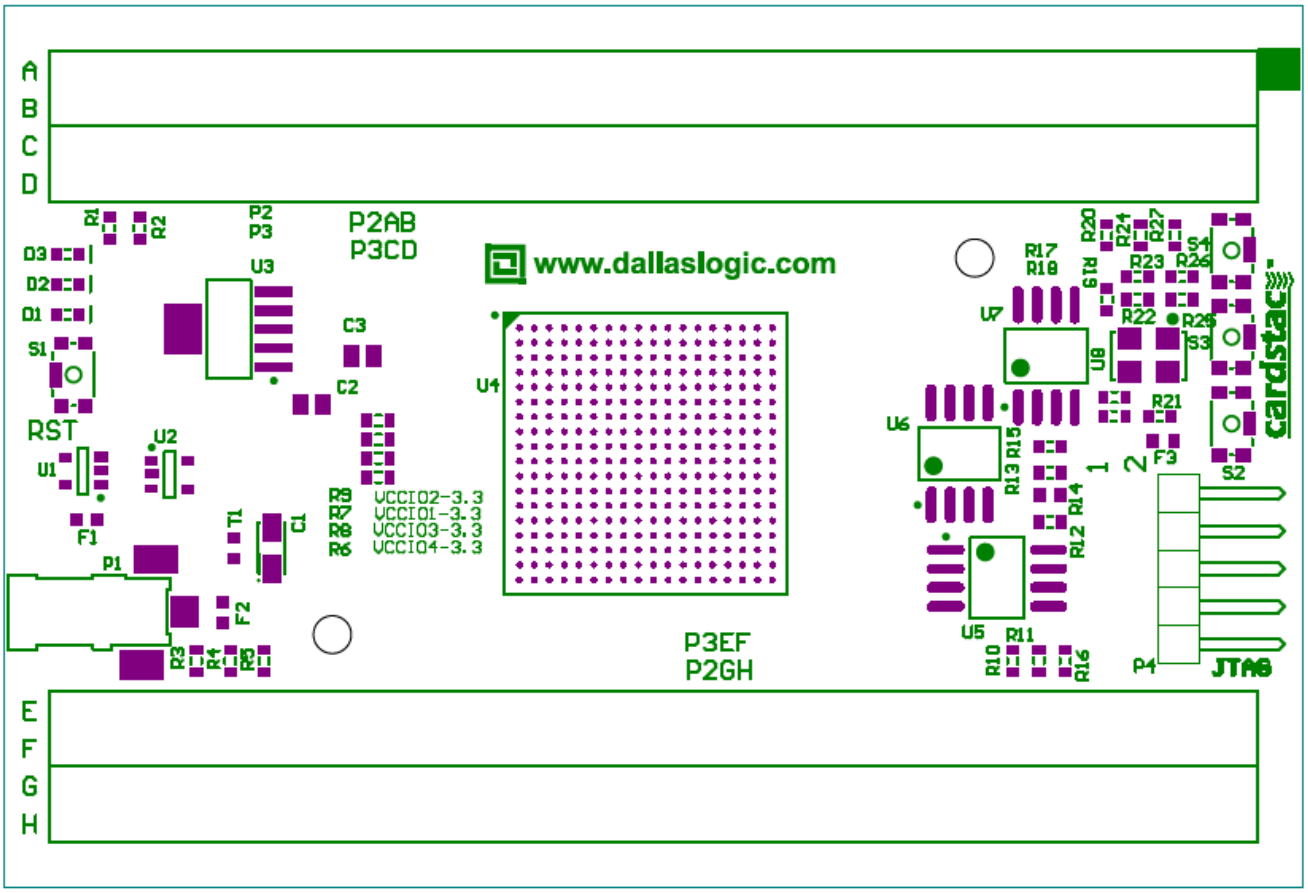

Figure 2-1 CMC5001 Silkscreen Image

The table below indicates the onboard components and their locations.

Table 2-1 Component Designators

Component Designator	Device
U4	Altera MAX V CPLD 5M2210ZF324C5N in 324 pin BGA package
P2AB, P3CD	Cardstac connector (32 pin)
P3EF, P2GH	Cardstac connector (32 pin)
U5,U6,U7	25AA1024 1Mbit EEPROM
U2	TC77 Temperature Sensor
U3	TPS73718 1.8V Power Regulator
D1,D2,D3	User LEDs
S2,S3,S4	User Switches
U8	25MHz Oscillator
S1	Board Reset Switch
P1	DC Jack Input power Connector
P4	JTAG Connector

3. Component Descriptions

5M2210ZF324C5N MAX V CPLD

The 5M2210ZF324C5N is an advanced, low power CPLD. The device has the following features:

- 2210 Logic Elements/Blocks, 1700 Macrocells, 8192 User Flash bits
- 4 Global clocks
- 271 User I/O
- 324-pin BGA

For more information consult the 5M2210ZF324C5N's datasheet and the MAX V Handbook located at the link below:

http://www.altera.com/literature/lit-max-v.jsp

Clocks

The CMC5001 module includes a single 25MHz oscillator. The oscillator serves as the reference clock for the 5M2210ZF324C5N MAX V device.

LED indicators

The CMC5001 module includes 3 LEDs that are connected to the MAX V.

User Switches

Three user switches are available on board and connected to the CPLD. The switches include pull-up and de-bounce circuitry.

Special Note: R21, R25 and R26 (CMC5001 Rev A schematic) Sheet 8, have been replaced.
Original Value: 10K ohm
Updated Value: 120 ohm
The REVB schematic will reflect this change. All modules are populated with 120 Ohm resistors prior to shipping.

25AA1024 1Mbit EEPROM

Three Microchip 1Mbit Serial EEPROMs (25AA1024) are available. The devices interface with the CPLD using a 4 wire SPI interface.

TC77 Temperature Sensor

The Microchip TC77 is a low power, ±1.0°C accurate temperature sensor. The device interfaces with the CPLD using a 3 wire SPI interface.

Cardstac Connectors

The CMC5001 module supports the CARDSTAC, Full size card, 64 pin dual row interfaces. This interface uses four 32 pin 0.1" pitch pin headers. The connectors are "stack-through" type connectors that provide both female (top) and male (bottom) gender.

The CARDSTAC interface specification can be found here:

http://www.dallaslogic.com/prod_cardstac_files/cardstac_spec_ver2_11.pdf

Power Input

WARNING

Do not directly connect 5V IO based devices to the CMC5001's IO pins. Always use a 5V translator IC.

WARNING

Do not connect an external +3.3V power supply to DC Jack P1 if you have 3.3V attached to any 3.3V Cardstac header pin from a secondary power source

The CMC5001 module can accept 3.3V input voltage via pins B31,H1,A32,G2,C2,E32,F31, and D1 (+3.3V) of headers P3 and P4. These pins can be used to input power to the module, or if the DC JACK is attached to the module, then these pins can provide power to external circuits. Do not connect an external +3.3V power supply to DC Jack P1 if you have 3.3V attached to these pins from another power source. The current limit for pin group A32/B31/E32/F31 is 3 Amperes, and the current limit for pin group C2/D1/G2/H1 is also 3 Amperes. Current drawn from the group must not exceed the limit. Each pin group is fused with a 3 Ampere fuse. The module's +3.3V power rail is designed to **operate at 3.14 – 3.46V** (3.3V +/-5%).

4. Hardware Setup

CMC5001 Module Setup

Steps to setup and run your CMC5001 module are:

1. Place the CMC5001 module on your bench area so as to not short any of the pins on the PCB.

2. Power can be applied to the module using the 0.65mm DC jack (P1), or power can be applied using the designated 3.3V Cardstac header pins.

3. Connect an Altera USB Blaster to the 10 pin JTAG connector labeled P4. Verify that the PIN 1 indicator on the USB Blaster is correctly aligned with PIN 1 indicator of the JTAG connector (P4).

4. Open the QII programmer from the Altera Quartus II design tool. The Quartus II programmer is located under the "Tools" pull down menu located at the top of the menu bar.

5. With the QII programmer open, click the Auto Detect button. If the module is connected correctly to the programmer the tool should return with the 5M2210ZF324C5N identified as the device.

6. With the 5M2210ZF324C5N identified, click the change file button and select the design file for download. Be sure to place a check mark in the program/configure column. Press the Start button to initiate the programming sequence.

5M2210 Bank Power Selection

The CMC5001 is designed to allow selectable Bank IO power. The device can be configured for either 1.8V or 3.3V operation for three of the four IO banks. All of the IO banks are configured for 3.3V operation during manufacturing. VCCIO3 (3.3V) is non-configurable because this bank supplies the on-chip JTAG configuration circuit. A zero ohm resistor (R8) can be removed which will disconnect power from VCCIO3, however this is not recommended.

VCCIO1, VCCIO2 and VCCIO3 are configurable for either 3.3V or 1.8V operation via resistor substitution. The following table identifies the required resistor modifications for a given VCCIO power rail.

Table 4-1 VCCIO power selection

BANK	3.3V Operation	1.8V Operation
VCCIO1	R7 = 0 ohm, R33 = 10M ohm	R7 = 10m ohm, R33 = 0 ohm
VCCIO2	R9 =0 ohm, R34 = 10M ohm	R9 =10M ohm, R34 = 0 ohm
VCCIO3	R8 =0 ohm	Not Available
VCCIO4	R6 =0 ohm, R32 = 10M ohm	R6 =10M ohm, R32 = 0 ohm

Reference Design Schematic

CMC5001 schematic pages should be referenced for details on circuit design or when connecting devices to the supplied pin-headers. The schematic file (.pdf) is available for download from www.dallaslogic.com. The 5M2210ZF324C5N is located on page four and five of the schematic.

5. CMC5001 Starter Design

CMC5001 Starter Design File Install

The CMC5001 reference design is a hardware only solution composed of counters and state machines. The intent of the design is to provide a method for verifying the module's feature set. A brief discussion of the design is provided below.

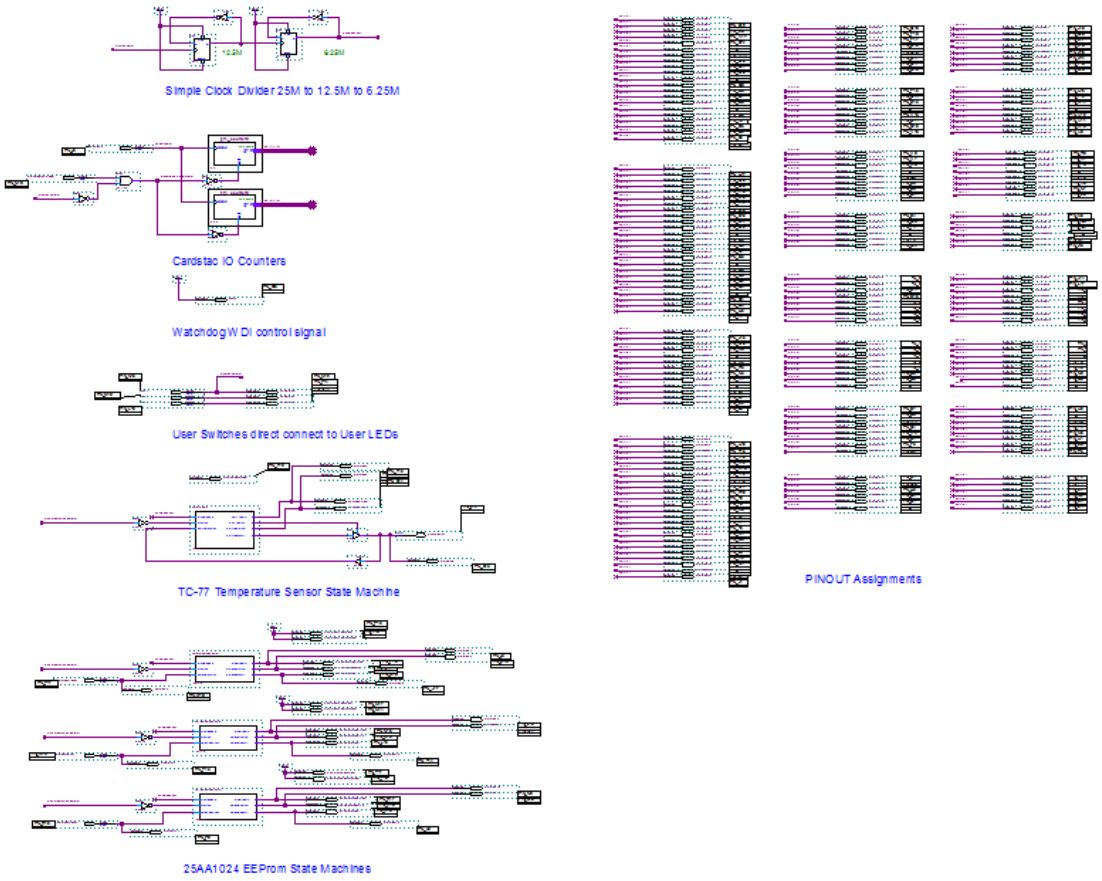

Figure 5-1 CMC5001 Reference Design BDF

The reference design is composed of seven elements. These items include a simple clock divider circuit, IO counters, watchdog control bit, user switches and LEDs, TC77 SPI state machine, three 25AA1024 (EEPROM) SPI state machines and the Cardstac IO pin assignments.

Simple Clock Divider:

The clock divider circuit is a simple two flip flop cascade circuit that provides clock division. The input clock to the module is 25Mhz. This circuit provides both a 12.5 Mhz. clock and a 6.25 Mhz. clock. This simple circuit is adequate for generating a clock to drive the SPI state machines. Use of a PLL would be a better choice if a high quality clock were required.

Cardstac IO counters:

The Cardstac IO counters are Altera Megafunctions. These counters are defined as 8 bit up counters and are clocked with the modules 25 Mhz. clock. The output counter bits are fed to the Cardstac IO as a stimulus source . This allowed unique data to be provided to the pin headers for verification using a logic analyzer.

Watchdog WDI control bit:

The WDI control bit is available for control of the TPS3820 watchdog feature. This function has been verified on the module, however the current reference design places a logic high on this control bit, thus disabling the watchdog function.

User Switches and LEDs:

The reference design routes the three input pushbutton switches (S2, S3, S4) labeled SW1, SW2 and SW3 in the reference design directly to the modules status LEDs (D1, D2, D3).

Table 5-1 Switch to LED connection matrix

Switch Designator	Ref Design Label	LED Designator	Ref Design Label
S2	SW1	D3	LED_RED
S3	SW2	D2	LED_YEL
S4	SW3	D1	LED_GRN

TC-77 Temperature Sensor State machine:

The TC-77 state machine is designed to read the manufacturer's id from the TC-77 device. The following procedure is implemented in the state machine:

1. Drive CS low to initiate the communication cycle.
2. Read 16 bits of temperature data from the Temperature register.
3. Write 16 bits of data (i.e. XXFF hex) to the Configuration register to enter Shutdown mode.
4. Read the 16 bits from the Manufacturer's ID register (C15:C8 = 54 hex) to verify that the sensor is a Microchip device.
5. Write 8 to 16 bits of data FFFF hex to enter Continuous Conversion Mode.
6. Return CS high to terminate the communication cycle.

The manufacturer's ID was verified with a Logic Analyzer attached to the SPI interface.

25AA1024 EEprom State machine:

The 25AA1024 state machine is designed to read the manufacturer's id from the 25AA1024 device. Three machines are implemented to communicate with each of the three on module 25AA1024 devices. The following procedure is implemented in the state machine:

1. Drive CS low to initiate a release from deep power-down mode and read electronic signature ID.

2. Write the RDID Instruction code "10101011".
3. Write a 24bit dummy address.
4. After the last bit of the dummy address is clocked in, the 8-bit electronic ID is clocked out
5. Return CS high to terminate the communication cycle.

The manufacturer's ID was verified with a Logic Analyzer attached to the SPI interface.

Cardstac IO Pin Assignments:

The Reference design provides all of the available IO assignments for connecting the CPLD to the module's external pin headers.

Mechanical Dimensions

The mechanical dimensions for the CMC5001 module are shown in the diagram below.

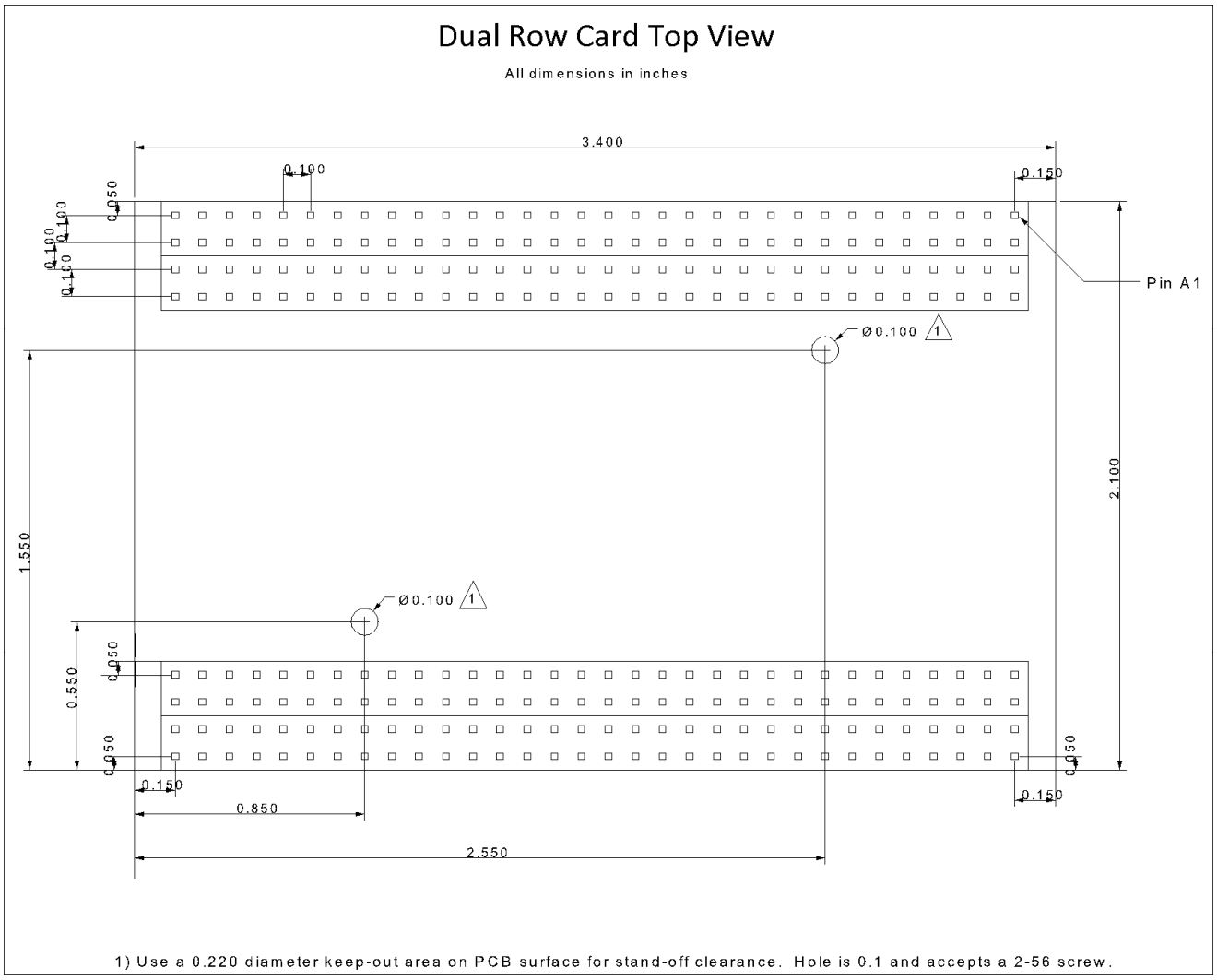

Figure 5-2 CMC5001 Mechanical Diagram

6. Ordering and Technical Help

Ordering Information

CMC5001 modules and related products can be ordered directly from our website at www.dallaslogic.com. Orders can be shipped to almost any destination in the world. Shipping costs can be obtained on the website before the order is finalized (submitted).

CMC5001 Module Technical Help

The best way to obtain help with problems is to email us at support@dallaslogic.com. We generally reply within 24hrs of receiving an inquiry or request for help with problems that are related to the operation of your MAX V module. Before contacting us with inquiries, please make sure you have:

1. Verified fuses F1 , F2, and F3 and checked the +3.3V input level at header pins.
2. Remove any test circuits connected to the CMC5001 PCB and restore it to its original design state.
3. Re-program and test your CMC5001 module with the original reference design load.

For questions related specifically to Altera's MAX V devices, please refer to Altera's documentation or online support web pages.

Warranty Information

Your un-modified CMC5001 assembly is guaranteed to be free of defects in material and workmanship for a period of ninety days from the date of purchase. If your CMC5001 module stops working during the ninety-day period, and is in its original, un-modified state, first contact us at support@dallaslogic.com. If the problem cannot be resolved, you must return the PCB assembly and power supply, postage prepaid to Dallas Logic Corporation. All repairs and return ship will be made within 10 days of receipt of package. During the warranty period, Dallas Logic will, at its option, repair, replace, or refund the purchase price. Products that have been damaged or modified from their original design state are not covered by warranty. No warranty is implied with respect to the software or firmware files.

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