Design Notes

FID1 FID2 LOGO1

FID3 FID4

1) EP3C25 device symbol has been pin swapped. DO NOT UPDATE EP3C25 SCHEMATIC SYMBOL FROM LIBRARY!

2) CMCS002M is configured as a Cardstac master card.

3) Carstac header pins G8-G15 (8 pins) are shared with SRAM device for use as data bus pins. Set SRAM device CE- pin high to disable the SRAM device (pin L4 of FPGA device tied to VCC inside FPGA design).

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REVISION TABLE

05-15-09	A	ET	Initial release of the schematic.

Title	*Cardstac Cntlr., Std. Size, Altera EP3C25*		Dallas Logic Corporation 2300 McDermott Rd. #200-305 Plano TX 75025 USA
Size: B	Number: CMCS002M	Revision: A	
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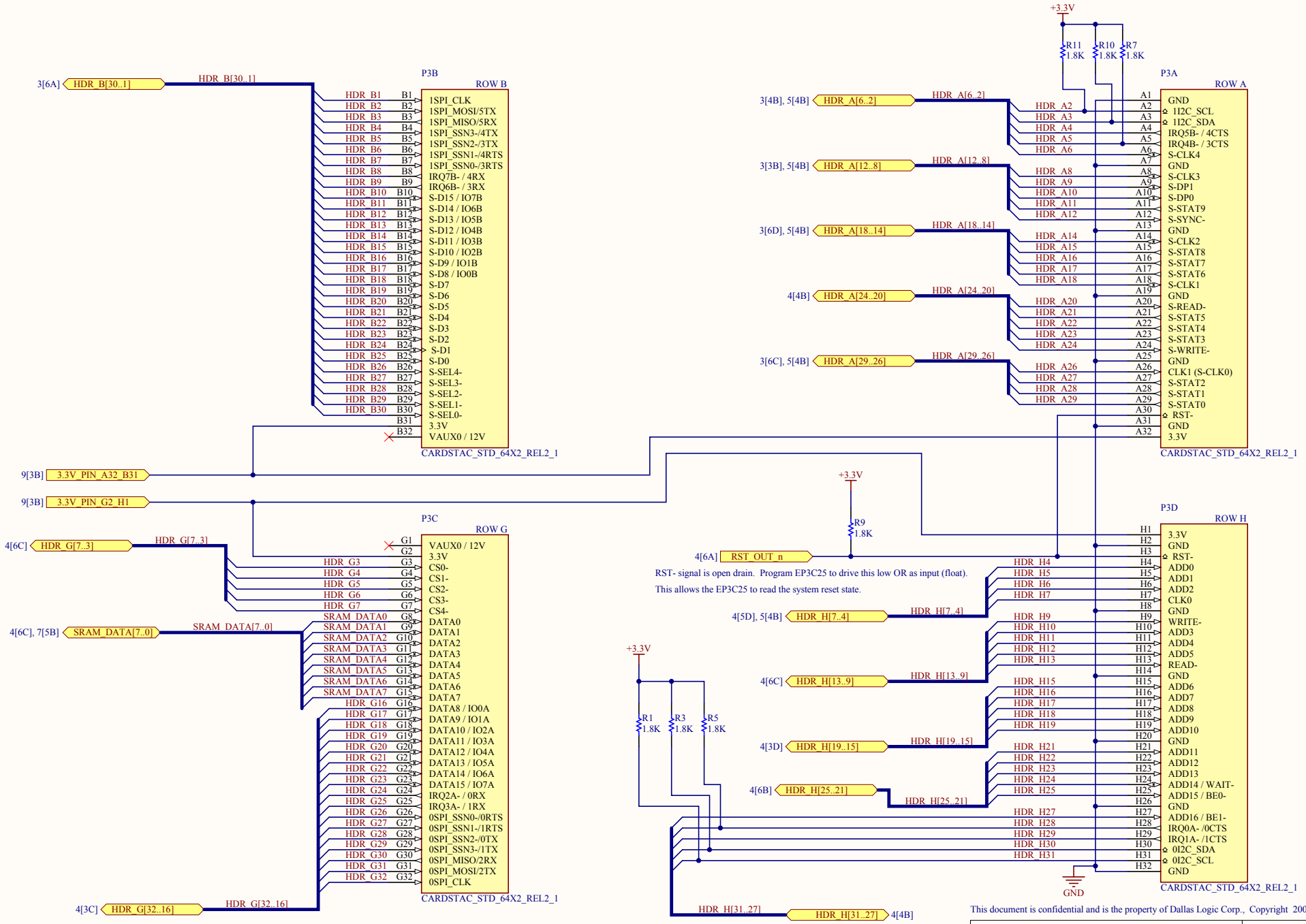

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Size: B	Number: CMCS002M	Revision: A	
Date: 5/15/2009	Time: 11:41:34 PM	Sheet 2 of 9	
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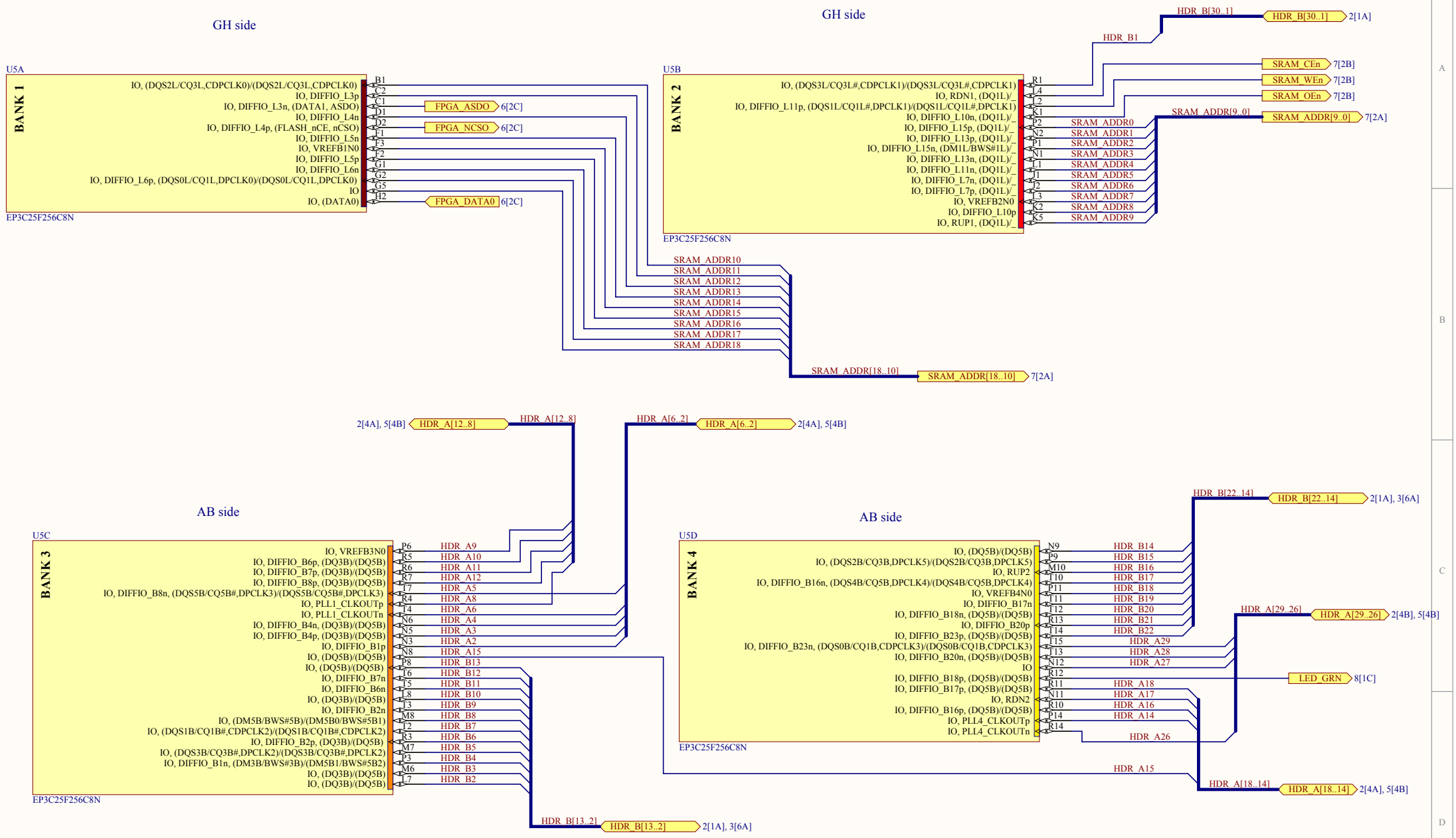
GH side
U5A
BANK 1
IO, (DQS2L/CQ3L,CDPCLK0)/(DQS2L/CQ3L,CDPCLK0)
IO, DIFFIO_L3p
IO, DIFFIO_L3n, (DATA1, ASDO)
IO, DIFFIO_L4n
IO, DIFFIO_L4p, (FLASH_nCE, nCSO)
IO, DIFFIO_L5n
IO, VREFB1N0
IO, DIFFIO_L5p
IO, DIFFIO_L6n
IO, DIFFIO_L6p, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)
IO
IO, (DATA0)
B1
C2
C1
D1
D2
F1
F3
F2
G1
G2
G5
H2
FPGA_ASDO
6[2C]
FPGA_NCSO
6[2C]
FPGA_DATA0
6[2C]
EP3C25F256C8N
GH side
U5B
BANK 2
IO, (DQS3L/CQ3L#,DPCLK1)/(DQS3L/CQ3L#,DPCLK1)
IO, RDN1, (DQ1L)/_
IO, DIFFIO_L11p, (DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)
IO, DIFFIO_L10n, (DQ1L)/_
IO, DIFFIO_L15p, (DQ1L)/_
IO, DIFFIO_L13p, (DQ1L)/_
IO, DIFFIO_L15n, (DM1L/BWS#1L)/_
IO, DIFFIO_L13n, (DQ1L)/_
IO, DIFFIO_L11n, (DQ1L)/_
IO, DIFFIO_L7n, (DQ1L)/_
IO, DIFFIO_L7p, (DQ1L)/_
IO, VREFB2N0
IO, DIFFIO_L10p
IO, RUP1, (DQ1L)/_
R1
L4
L2
K1
P2
N2
P1
N1
L1
J1
J2
K3
K2
K5
HDR_B[30..1]
HDR_B1
SRAM_CEn
SRAM_WEn
SRAM_OEn
SRAM_ADDR[9..0]
SRAM_ADDR0
SRAM_ADDR1
SRAM_ADDR2
SRAM_ADDR3
SRAM_ADDR4
SRAM_ADDR5
SRAM_ADDR6
SRAM_ADDR7
SRAM_ADDR8
SRAM_ADDR9
EP3C25F256C8N
SRAM_ADDR10
SRAM_ADDR11
SRAM_ADDR12
SRAM_ADDR13
SRAM_ADDR14
SRAM_ADDR15
SRAM_ADDR16
SRAM_ADDR17
SRAM_ADDR18
SRAM_ADDR[18..10]
HDR_B[30..1]
2[1A]
7[2B]
7[2B]
7[2B]
SRAM_ADDR[9..0]
7[2A]
SRAM_ADDR[18..10]
7[2A]
2[4A], 5[4B]
HDR_A[12..8]
HDR_A[12..8]
HDR_A[6..2]
HDR_A[6..2]
2[4A], 5[4B]
AB side
U5C
BANK 3
IO, VREFB3N0
IO, DIFFIO_B6p, (DQ3B)/(DQ5B)
IO, DIFFIO_B7p, (DQ3B)/(DQ5B)
IO, DIFFIO_B8p, (DQ3B)/(DQ5B)
IO, DIFFIO_B8n, (DQS5B/CQ5B#,DPCLK3)/(DQS5B/CQ5B#,DPCLK3)
IO, PLL1_CLKOUTp
IO, PLL1_CLKOUTn
IO, DIFFIO_B4n, (DQ3B)/(DQ5B)
IO, DIFFIO_B4p, (DQ3B)/(DQ5B)
IO, DIFFIO_B1p
IO, (DQ5B)/(DQ5B)
IO, (DQ5B)/(DQ5B)
IO, DIFFIO_B7n
IO, DIFFIO_B6n
IO, (DQ3B)/(DQ5B)
IO, DIFFIO_B2n
IO, (DM5B/BWS#5B)/(DM5B0/BWS#5B1)
IO, (DQS1B/CQ1B#,CDPCLK2)/(DQS1B/CQ1B#,CDPCLK2)
IO, DIFFIO_B2p, (DQ3B)/(DQ5B)
IO, (DQS3B/CQ3B#,DPCLK2)/(DQS3B/CQ3B#,DPCLK2)
IO, DIFFIO_B1n, (DM3B/BWS#3B)/(DM5B1/BWS#5B2)
IO, (DQ3B)/(DQ5B)
IO, (DQ3B)/(DQ5B)
P6
R5
R6
R7
T7
R4
T4
N6
N5
N3
N8
P8
T6
T5
L8
T3
M8
T2
R3
M7
P3
M6
L7
HDR_A9
HDR_A10
HDR_A11
HDR_A12
HDR_A5
HDR_A8
HDR_A6
HDR_A4
HDR_A3
HDR_A2
HDR_A15
HDR_B13
HDR_B12
HDR_B11
HDR_B10
HDR_B9
HDR_B8
HDR_B7
HDR_B6
HDR_B5
HDR_B4
HDR_B3
HDR_B2
EP3C25F256C8N
HDR_B[13..2]
HDR_B[13..2]
2[1A], 3[6A]
AB side
U5D
BANK 4
IO, (DQ5B)/(DQ5B)
IO, (DQS2B/CQ3B,DPCLK5)/(DQS2B/CQ3B,DPCLK5)
IO, RUP2
IO, DIFFIO_B16n, (DQS4B/CQ5B,DPCLK4)/(DQS4B/CQ5B,DPCLK4)
IO, VREFB4N0
IO, DIFFIO_B17n
IO, DIFFIO_B18n, (DQ5B)/(DQ5B)
IO, DIFFIO_B20p
IO, DIFFIO_B23p, (DQ5B)/(DQ5B)
IO, DIFFIO_B23n, (DQS0B/CQ1B,CDPCLK3)/(DQS0B/CQ1B,CDPCLK3)
IO, DIFFIO_B20n, (DQ5B)/(DQ5B)
IO
IO, DIFFIO_B18p, (DQ5B)/(DQ5B)
IO, DIFFIO_B17p, (DQ5B)/(DQ5B)
IO, RDN2
IO, DIFFIO_B16p, (DQ5B)/(DQ5B)
IO, PLL4_CLKOUTp
IO, PLL4_CLKOUTn
N9
P9
M10
T10
R11
T11
T12
R13
T14
T15
T13
N12
R12
R11
N11
R10
P14
R14
HDR_B14
HDR_B15
HDR_B16
HDR_B17
HDR_B18
HDR_B19
HDR_B20
HDR_B21
HDR_B22
HDR_A29
HDR_A28
HDR_A27
HDR_A18
HDR_A17
HDR_A16
HDR_A14
HDR_A26
EP3C25F256C8N
HDR_B[22..14]
HDR_B[22..14]
2[1A], 3[6A]
HDR_A[29..26]
HDR_A[29..26]
2[4B], 5[4B]
LED_GRN
8[1C]
HDR_A15
HDR_A[18..14]
HDR_A[18..14]
2[4A], 5[4B]
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Size: B
Number: CMCS002M
Revision: A
Date: 5/15/2009
Time: 11:41:34 PM
Sheet 3 of 9
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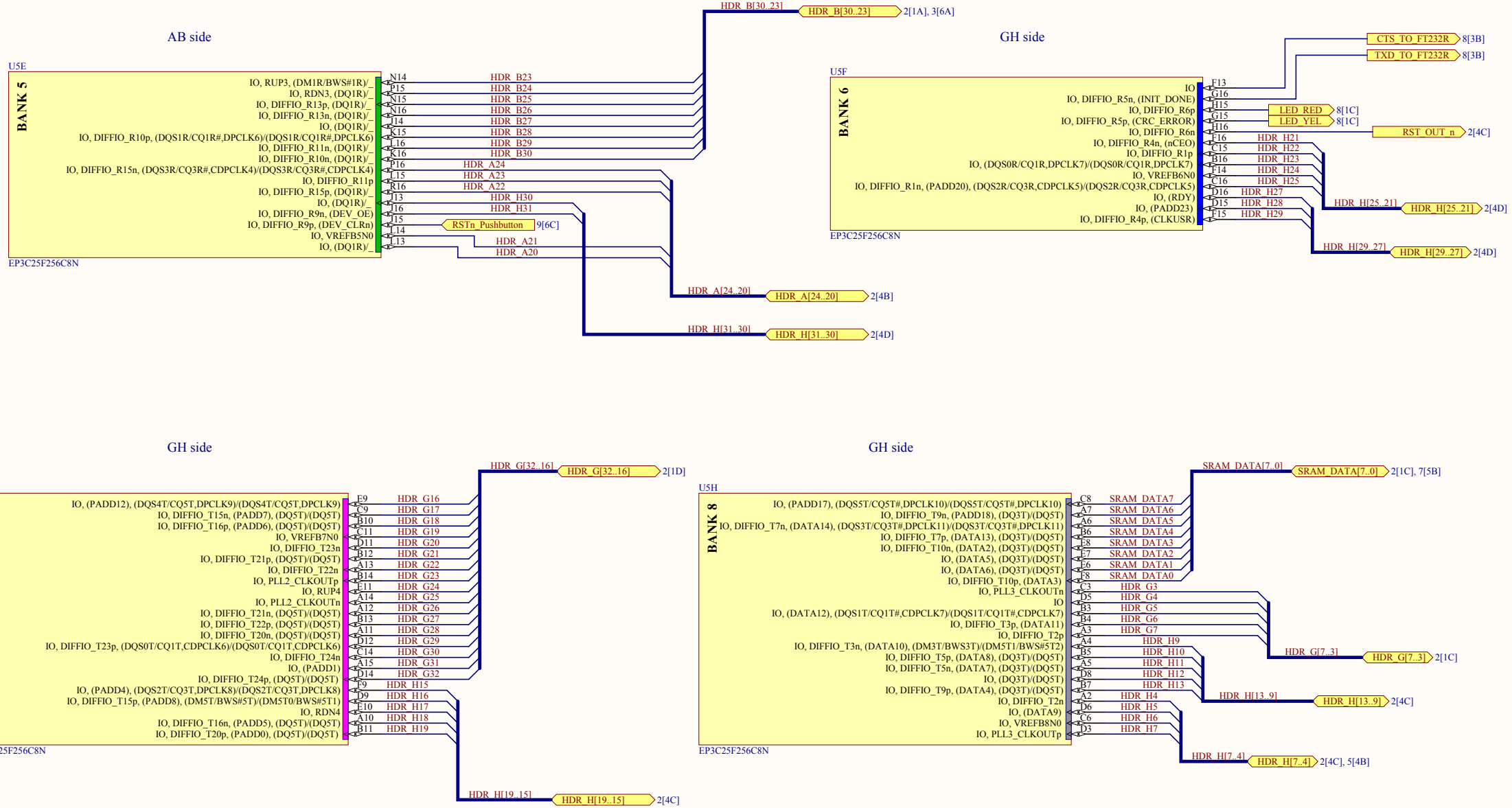
Dallas Logic Corporation
2300 McDermott Rd.
#200-305
Plano TX 75025 USA
Dallas Logic corporation


AB side
U5E
BANK 5
IO, RUP3, (DM1R/BWS#1R)/_
IO, RDN3, (DQ1R)/_
IO, DIFFIO_R13p, (DQ1R)/_
IO, DIFFIO_R13n, (DQ1R)/_
IO, (DQ1R)/_
IO, DIFFIO_R10p, (DQS1R/CQ1R#,DPCLK6)/(DQS1R/CQ1R#,DPCLK6)
IO, DIFFIO_R11n, (DQ1R)/_
IO, DIFFIO_R10n, (DQ1R)/_
IO, DIFFIO_R15n, (DQS3R/CQ3R#,CDPCLK4)/(DQS3R/CQ3R#,CDPCLK4)
IO, DIFFIO_R11p
IO, DIFFIO_R15p, (DQ1R)/_
IO, (DQ1R)/_
IO, DIFFIO_R9n, (DEV_OE)
IO, DIFFIO_R9p, (DEV_CLRn)
IO, VREFB5N0
IO, (DQ1R)/_
N14 HDR_B23
P15 HDR_B24
N15 HDR_B25
N16 HDR_B26
J14 HDR_B27
K15 HDR_B28
L16 HDR_B29
K16 HDR_B30
P16 HDR_A24
L15 HDR_A23
R16 HDR_A22
J13 HDR_H30
J16 HDR_H31
J15 RSTn_Pushbutton 9[6C]
L14 HDR_A21
L13 HDR_A20
EP3C25F256C8N
HDR_B[30..23] HDR_B[30..23] 2[1A], 3[6A]
HDR_A[24..20] HDR_A[24..20] 2[4B]
HDR_H[31..30] HDR_H[31..30] 2[4D]
GH side
U5F
BANK 6
IO
IO, DIFFIO_R5n, (INIT_DONE)
IO, DIFFIO_R6p
IO, DIFFIO_R5p, (CRC_ERROR)
IO, DIFFIO_R6n
IO, DIFFIO_R4n, (nCEO)
IO, DIFFIO_R1p
IO, (DQS0R/CQ1R,DPCLK7)/(DQS0R/CQ1R,DPCLK7)
IO, VREFB6N0
IO, DIFFIO_R1n, (PADD20), (DQS2R/CQ3R,CDPCLK5)/(DQS2R/CQ3R,CDPCLK5)
IO, (RDY)
IO, (PADD23)
IO, DIFFIO_R4p, (CLKUSR)
F13
G16
H15 LED_RED 8[1C]
G15 LED_YEL 8[1C]
H16 RST_OUT_n 2[4C]
E16 HDR_H21
C15 HDR_H22
B16 HDR_H23
F14 HDR_H24
C16 HDR_H25
D16 HDR_H27
D15 HDR_H28
E15 HDR_H29
EP3C25F256C8N
CTS_TO_FT232R 8[3B]
TXD_TO_FT232R 8[3B]
HDR_H[25..21] HDR_H[25..21] 2[4D]
HDR_H[29..27] HDR_H[29..27] 2[4D]
GH side
U5G
BANK 7
IO, (PADD12), (DQS4T/CQ5T,DPCLK9)/(DQS4T/CQ5T,DPCLK9)
IO, DIFFIO_T15n, (PADD7), (DQ5T)/(DQ5T)
IO, DIFFIO_T16p, (PADD6), (DQ5T)/(DQ5T)
IO, VREFB7N0
IO, DIFFIO_T23n
IO, DIFFIO_T21p, (DQ5T)/(DQ5T)
IO, DIFFIO_T22n
IO, PLL2_CLKOUTp
IO, RUP4
IO, PLL2_CLKOUTn
IO, DIFFIO_T21n, (DQ5T)/(DQ5T)
IO, DIFFIO_T22p, (DQ5T)/(DQ5T)
IO, DIFFIO_T20n, (DQ5T)/(DQ5T)
IO, DIFFIO_T23p, (DQS0T/CQ1T,CDPCLK6)/(DQS0T/CQ1T,CDPCLK6)
IO, DIFFIO_T24n
IO, (PADD1)
IO, DIFFIO_T24p, (DQ5T)/(DQ5T)
IO, (PADD4), (DQS2T/CQ3T,DPCLK8)/(DQS2T/CQ3T,DPCLK8)
IO, DIFFIO_T15p, (PADD8), (DM5T/BWS#5T)/(DM5T0/BWS#5T1)
IO, RDN4
IO, DIFFIO_T16n, (PADD5), (DQ5T)/(DQ5T)
IO, DIFFIO_T20p, (PADD0), (DQ5T)/(DQ5T)
E9 HDR_G16
C9 HDR_G17
B10 HDR_G18
E11 HDR_G19
D11 HDR_G20
B12 HDR_G21
A13 HDR_G22
B14 HDR_G23
E11 HDR_G24
A14 HDR_G25
A12 HDR_G26
B13 HDR_G27
A11 HDR_G28
D12 HDR_G29
C14 HDR_G30
A15 HDR_G31
D14 HDR_G32
C9 HDR_H15
D9 HDR_H16
E10 HDR_H17
A10 HDR_H18
B11 HDR_H19
EP3C25F256C8N
HDR_G[32..16] HDR_G[32..16] 2[1D]
HDR_H[19..15] HDR_H[19..15] 2[4C]
GH side
U5H
BANK 8
IO, (PADD17), (DQS5T/CQ5T#,DPCLK10)/(DQS5T/CQ5T#,DPCLK10)
IO, DIFFIO_T9n, (PADD18), (DQ3T)/(DQ5T)
IO, DIFFIO_T7n, (DATA14), (DQS3T/CQ3T#,DPCLK11)/(DQS3T/CQ3T#,DPCLK11)
IO, DIFFIO_T7p, (DATA13), (DQ3T)/(DQ5T)
IO, DIFFIO_T10n, (DATA2), (DQ3T)/(DQ5T)
IO, (DATA5), (DQ3T)/(DQ5T)
IO, (DATA6), (DQ3T)/(DQ5T)
IO, DIFFIO_T10p, (DATA3)
IO, PLL3_CLKOUTn
IO
IO, (DATA12), (DQS1T/CQ1T#,CDPCLK7)/(DQS1T/CQ1T#,CDPCLK7)
IO, DIFFIO_T3p, (DATA11)
IO, DIFFIO_T2p
IO, DIFFIO_T3n, (DATA10), (DM3T/BWS3T)/(DM5T1/BWS#5T2)
IO, DIFFIO_T5p, (DATA8), (DQ3T)/(DQ5T)
IO, DIFFIO_T5n, (DATA7), (DQ3T)/(DQ5T)
IO, (DQ3T)/(DQ5T)
IO, DIFFIO_T9p, (DATA4), (DQ3T)/(DQ5T)
IO, DIFFIO_T2n
IO, (DATA9)
IO, VREFB8N0
IO, PLL3_CLKOUTp
C8 SRAM_DATA7
A7 SRAM_DATA6
A6 SRAM_DATA5
B6 SRAM_DATA4
E8 SRAM_DATA3
E7 SRAM_DATA2
E6 SRAM_DATA1
F8 SRAM_DATA0
C3 HDR_G3
D5 HDR_G4
B3 HDR_G5
B4 HDR_G6
A3 HDR_G7
A4 HDR_H9
B5 HDR_H10
A5 HDR_H11
D8 HDR_H12
B7 HDR_H13
A2 HDR_H4
D6 HDR_H5
C6 HDR_H6
D3 HDR_H7
EP3C25F256C8N
SRAM_DATA[7..0] SRAM_DATA[7..0] 2[1C], 7[5B]
HDR_G[7..3] HDR_G[7..3] 2[1C]
HDR_H[13..9] HDR_H[13..9] 2[4C]
HDR_H[7..4] HDR_H[7..4] 2[4C], 5[4B]
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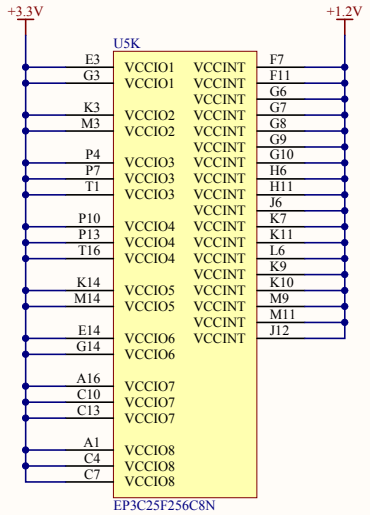
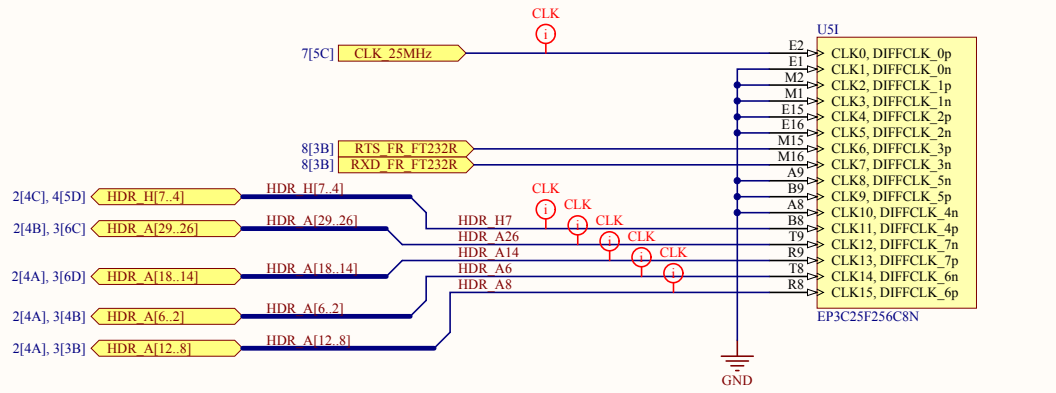
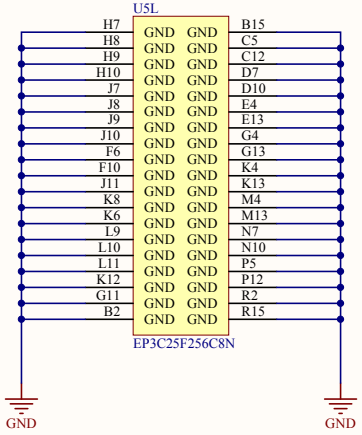
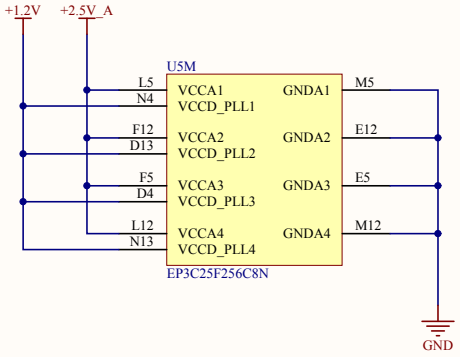
Dallas Logic corporation

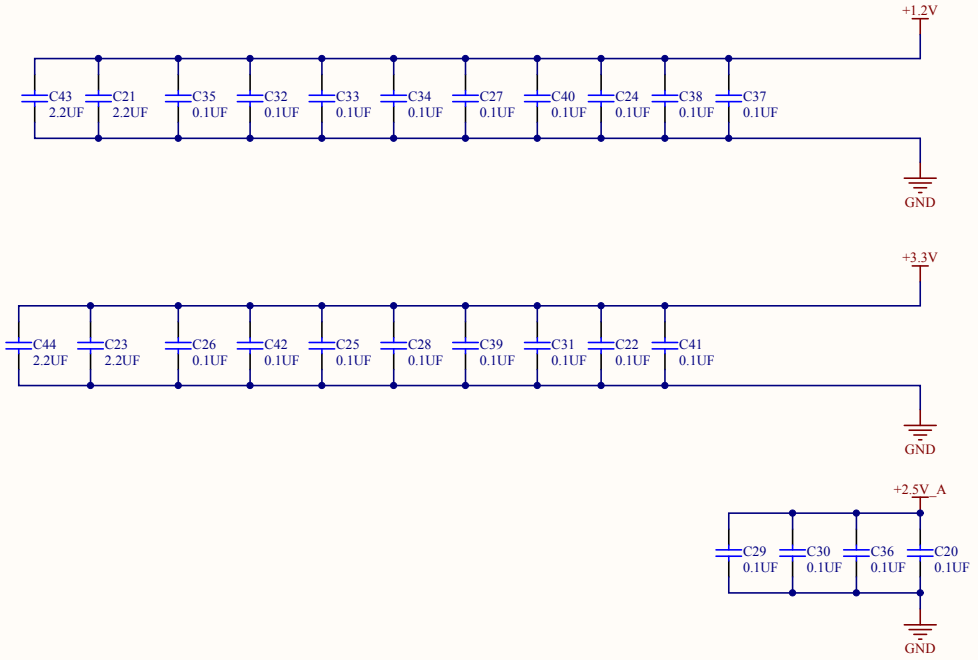




Per EP3C25 pin-out document, tie unused clocks to GND.







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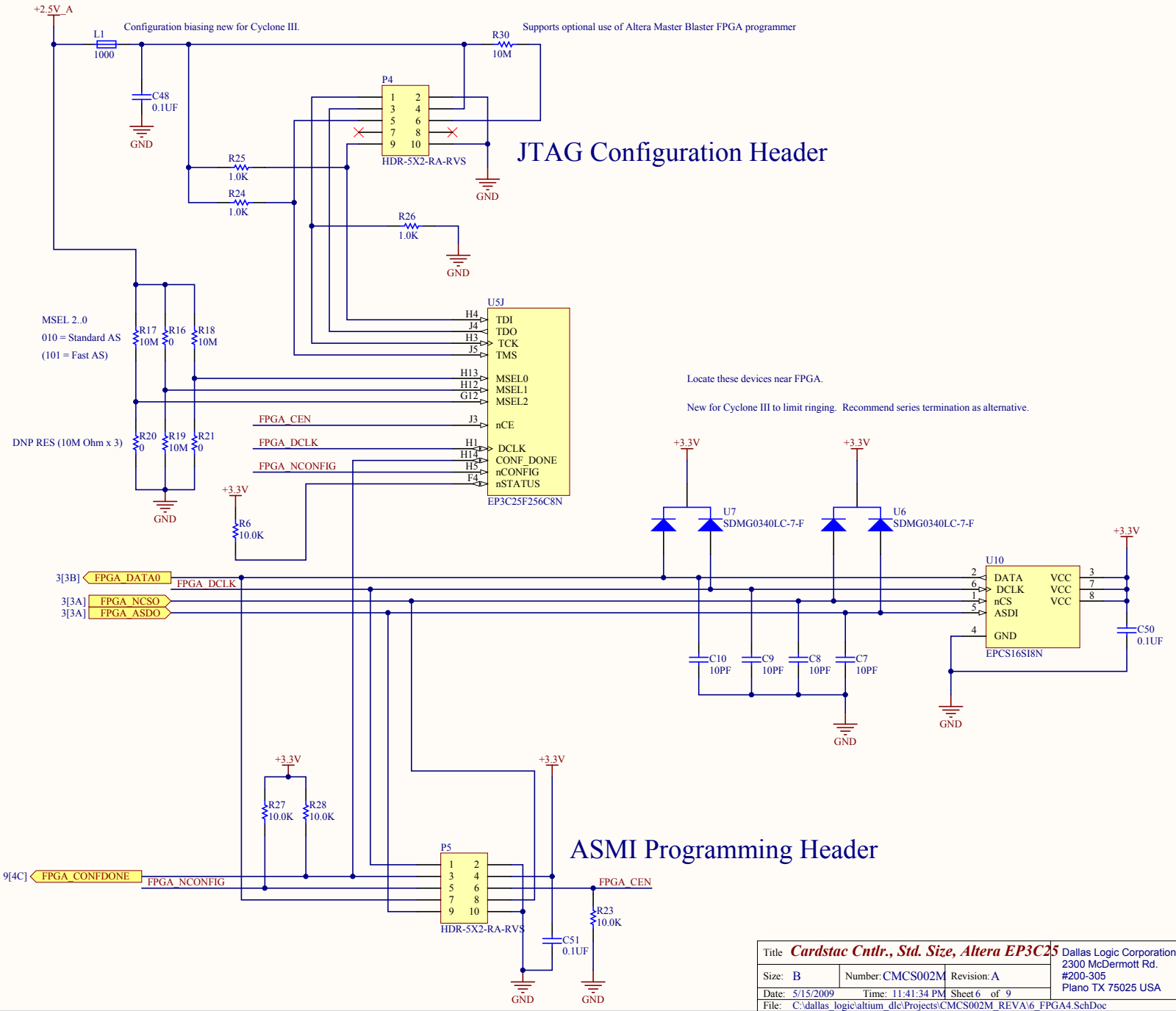

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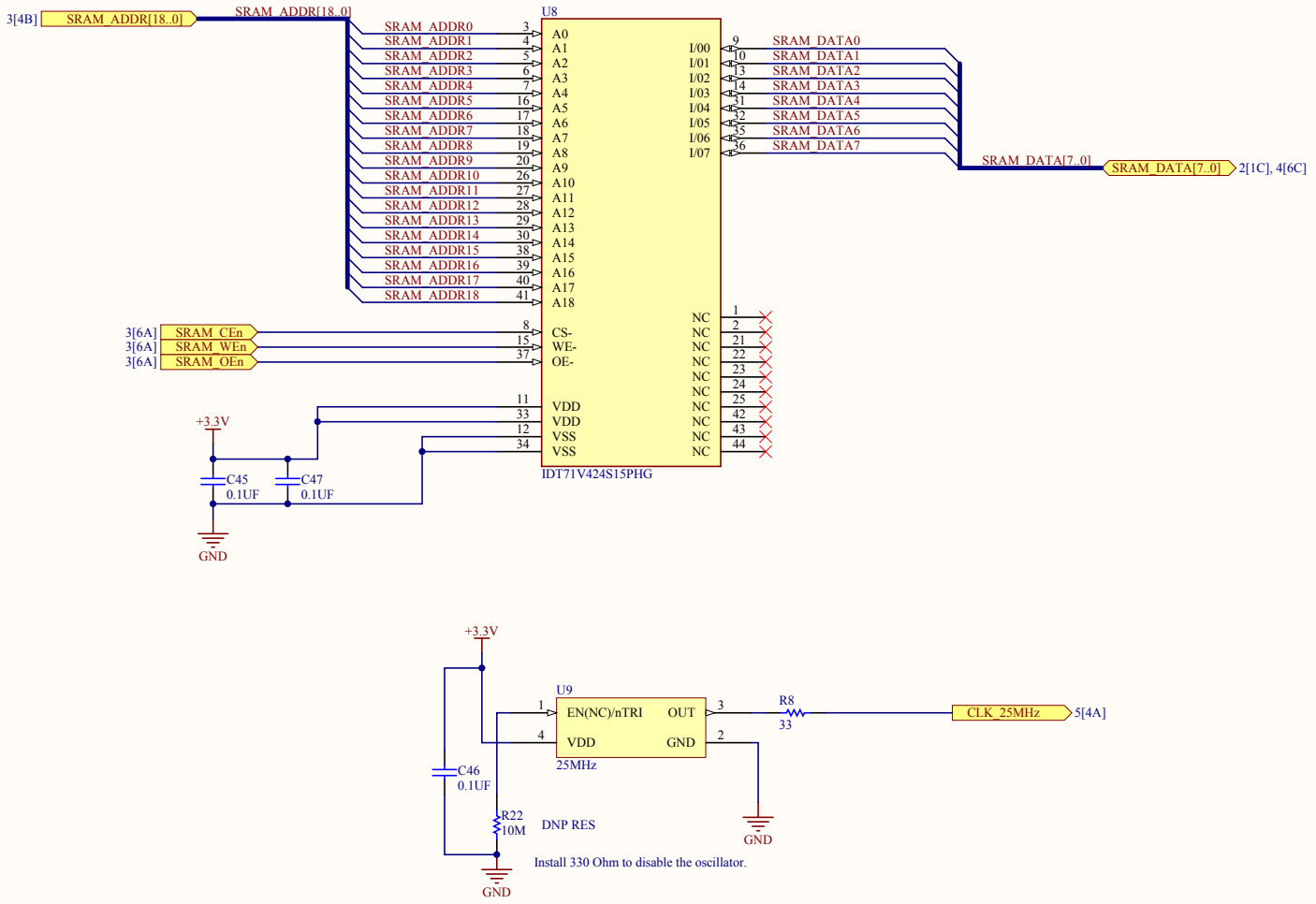
Dallas Logic Corporation
2300 McDermott Rd.
#200-305
Plano TX 75025 USA

512KX8 SRAM



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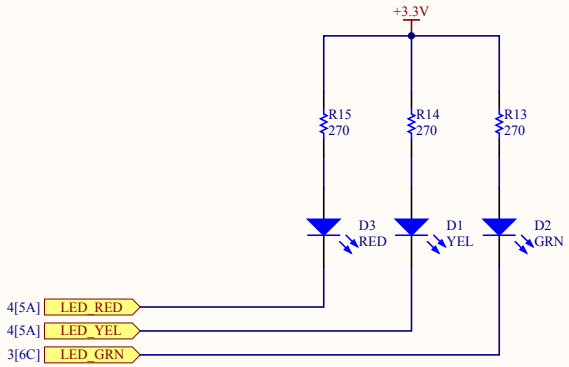
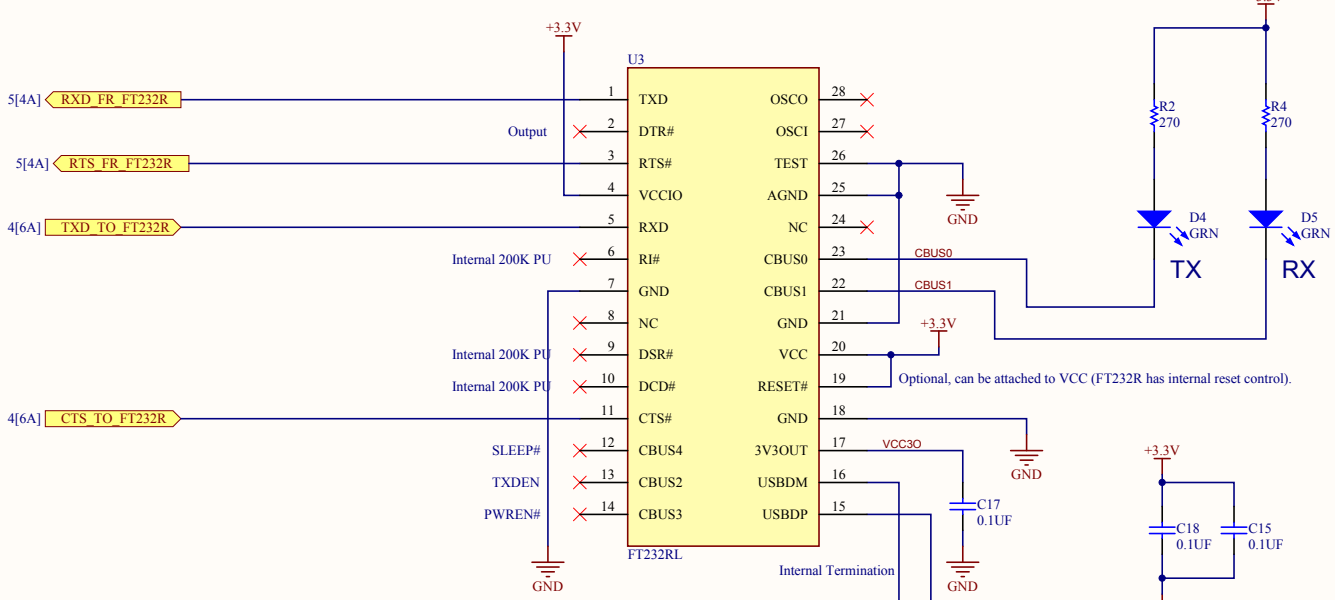
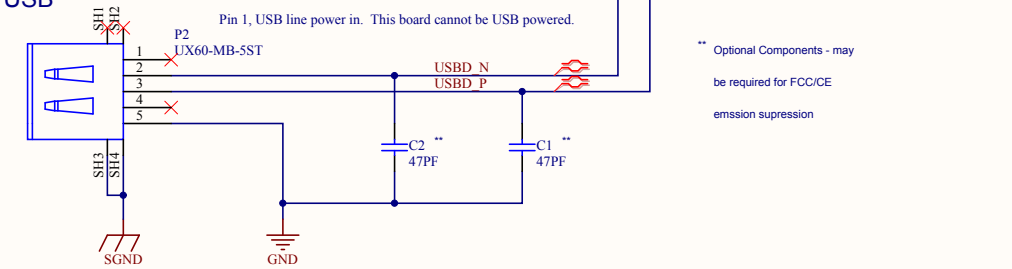
Status LEDS



FT232R USB TO UART SERIAL ADAPTOR



USB



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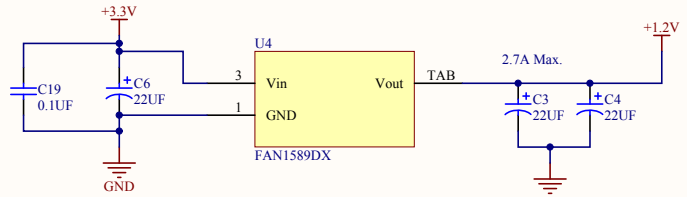
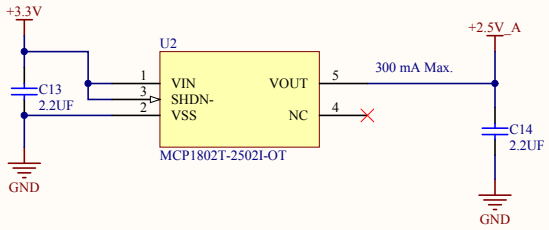
File: C:\dallas_logic\altium_dlc\Projects\CMCS002M_REVA\8_MISC.SchDoc			

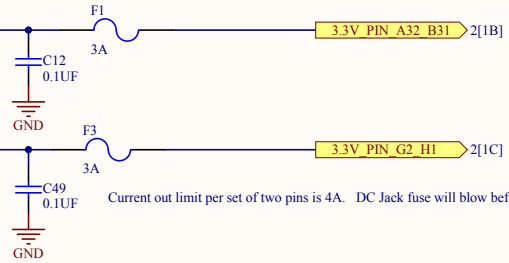
POWER SUPPLY





Remove fuses if other card in stack sources 3.3V power rail and local DCJACK is attached and powered (should not do this).

May also pull current in from 3.3V pin (local power from external source).

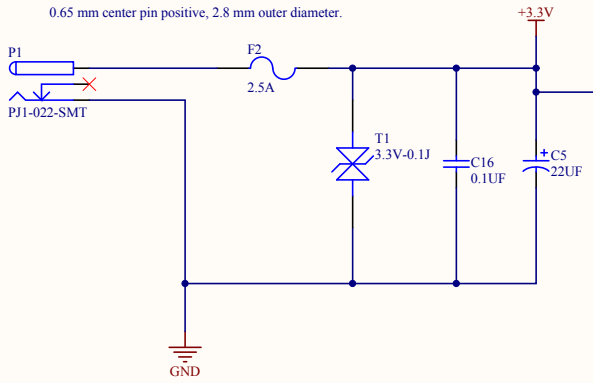


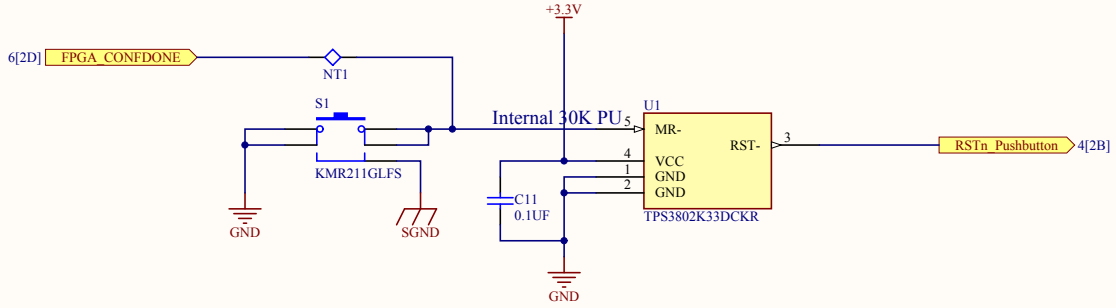
Current out limit per set of two pins is 4A. DC Jack fuse will blow before these will.

DC JACK

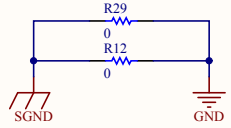
INPUT: +3.3V, 2.5A Max.

0.65 mm center pin positive, 2.8 mm outer diameter.





SGND (Shield GND or guard ring) connected to ground power pins at two corners of module.



Title	*Cardstac Cntlr., Std. Size, Altera EP3C25*	Dallas Logic Corporation 2300 McDermott Rd. #200-305 Plano TX 75025 USA	
Size: B	Number: CMCS002M	Revision: A	
Date: 5/15/2009	Time: 11:41:34 PM	Sheet 9 of 9	
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