

Quicgate_3c25 Reference Design Instructions

Special Note for 9.0 and 9.0 SP1 Users

Post from the NIOS FORUM:

It seems that with the 9.0 NIOS IDE, the Flash programmer doesn't put the software correctly in the EPCS device when used with a Cyclone III, preventing the NIOSII from booting. This is not corrected in SP1, but should in SP2. There is a thread on the subject in the NIOS forum.

http://alteraforum.com/forum/showthread.php?t=5547

The behavior of this bug is that NIOSII on Cyclone III does not boot up from EPCS if you programmed the SOF and ELF with the v9.0 Flash Programmer.

The workaround: replace 90\nios2eds\bin\sof2flash.jar with 81\nios2eds\bin\sof2flash.

Tool version: QUARTUS II 9.0 sp 2 / NIOSII IDE 9.0

- Download the reference design zip file from <u>www.dallaslogic.com</u>. Be sure to select the design that matches the module you purchased. i.e. Quicgate_3C25.
- Unzip the reference design to a target directory. Verify that the maintain directory structure setting is enabled for the unzip procedure.
- Launch the Quartus II software.
- On the top menu bar click the Project pulldown and select Restore Archived Project.
- Navigate to the *.qar and select it.
- The De-Archive procedure will rename the project directory with a "restored" suffix. In order to maintain the original directory tree, omit the name with the "restored" suffix. See below:

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Restore Archived Project	×
Archive name:	
ogic/Quicgate_Niomite/QII90/quicnios_3C25/quicnios_3c25.qar	
Show Log	
Destination folder:	
uicgate_Niomite/QII90/quicnios_3C25/quicnios_3c25	
Overwrite any existing files in the destination folder.	
OK Cancel	

Figure 1. Restored Archive Project

- Copy all of the directories found in the original unzipped directory to the newly created archive directory.
- The Quicgate Nios II project should now be available.
- The Software directory contains two directories: quicnios_3C25_demo and quicnios_3c25_syslib
- Lauch the NIOSII IDE. Take all of the default settings if prompted.
- Navigate to the FILE >> Import >> Existing Altera Nios II project. Now browse to the target directory containing the newly unzipped software directory. Now push into the software directory and left click the design directory. i.e quicnios_3c25_demo
- This project should now appear in the left window under the C/C++ Projects window.
- Now that the design file has been imported repeat the above steps and import the associated system library. The system library is located in the software directory and include either syslib or system_library in it's name.
- After importation the system library should now appear in the left window under the C/C++ Projects window.
- Before you can build, highlight the quicnios design in the IDE, click the right mouse button and select properties. Under the Associated system library tab, select the newly imported system library.
- Open the associated system library, and select the system library properties.
- Verify that the system library is configured like the system library shown in Figure 2.

Properties for quicnio	s_3c25_syslib			
type filter text	System Library			⇔ • ⇔ •
Info Builders C/C++Build C/C++Documentation C/C++File Types C/C++Indexer C/C++Indexer C/C++Indexer C/C++Project Paths Project References Refactoring History System Library	Target Hardware SOPC Builder System: CPU: cpu_0 System Library Contents RTOS: RTOS Options stdout: stdout: stdout: stderr: stdin: System dock timer: Timestamp timer: Max file descriptors: Program never exits V Support C++ Lightweight device driver API Link with profiling library Unimplemented instruction handler Software Components	Quicgate_Niomite\QII90\quicnios_3C25\quic none (single-threaded) uart uart uart uart imer 32 Clean exit (flush buffers) Reduced device drivers Small C library ModelSim only, no hardware support Run time stack checking	unker Script O Custom linker script none O Use auto-generated linker script Program memory (.text): Read-only data memory (.rodata): Read-only data memory (.rodata): Heap memory: Stack memory: Use a separate exception stack Exception stack memory: Maximum exception stack size (bytes):	Browse Select cy7c1049cv33 cy7c1049cv33 cy7c1049cv33 cy7c1049cv33 vector vector vector
<			Help Res	tore Defaults Apply
0			C	OK Cancel

Figure 2. System library Properties

• Now under Tools select the QII programmer. Select JTAG as the programming method and select the .sof file from the newly dearchived FPGA design. Select the program box and push the run button.

The New FLASH Programmer requires that you download the .sof file from the FPGA design prior to running the FLASH programmer. If the .sof file is not downloaded prior to programming, the FLASH programmer will fail to complete.

- Once programmed, launch the flash programmer also located under the Tools directory. Be sure that your new project is highlighted in the C++ projects window(left hand side of the IDE window) prior to launching the Flash Programmer.
- The first time the flash programmer is launched, you will need to create a new configuration. This can be achieved by selecting the NEW button located in the bottom left of the flash programmer window. If your project was highlighted in the C++ projects window prior to lauching the flash programmer then your new project should now be listed in the flash programmer configurations window.
- Complete the setup by editing your configuration to look like the one shown in Figure 2.
- Be sure to select the appropriate JTAG programming interface and hit the program button.
- YOU HAVE NOW FLASHED the Quicgate board.

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💽 Flash Programmer			
Program project to flash memory on target boa Program flash with quicnios_3c25 and top.sof (using script C:/di	rd allaslogic/Quicgate_Nomite/QI190/quicnios_3C25/software/quicnios_3c25_demo/Debug/quicnios_3c25_programmer.sh).		
Image: Control of the second secon	Name: quichios_3c25 programmer Main Target Connection Target Board: CYCLONEIII <no board="" builder="" in="" sopc="" specified="" system="" target="" the=""> Program software project into flash memory Project:</no>		
	quintios_3225 Nios IT ELP Executable: Debugiquintions_3225.elf Target Hardware SOPC Builder System PTF File: CPU: Additional nios2-flash-programmer arguments: Load JDI File VProgram FPGA configuration data into hardware image region of flash memory FPGA Configuration (SDF): Clailaislogic(Quicgate_Nomite(QI100/quicnios_3C25\top.sof Hardware Image: Custom Venory: epsc_flash_controller Offset: 0) e	
	File: Brows Memory: jepss_flash_controller Validate Nos II system ID before software download Apply Rev	e	
0	Program Flash C	lose	

Figure3. Flash Programmer

More Questions? Use the Dallas Logic Forums located at http://www.dallaslogic.com/forum/default.asp

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