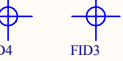


## Design Notes

1) PCB initially tested with ADC34J45 AD device (160 MSPS, 14 bit). Several variants of the ADC34JXX family will work with this PCB.



### TABLE OF CONTENTS:

- 1- Cover sheet
- 2- HSMC connector Bank1 and Bank2
- 3- HSMC connector Bank3
- 4- Quad analog to digital converter, JESD204B
- 5- Clock circuits
- 6- Clock circuits, LMK04826
- 7- Front end, AC coupled
- 8- Front end, DC coupled
- 9- Power supply

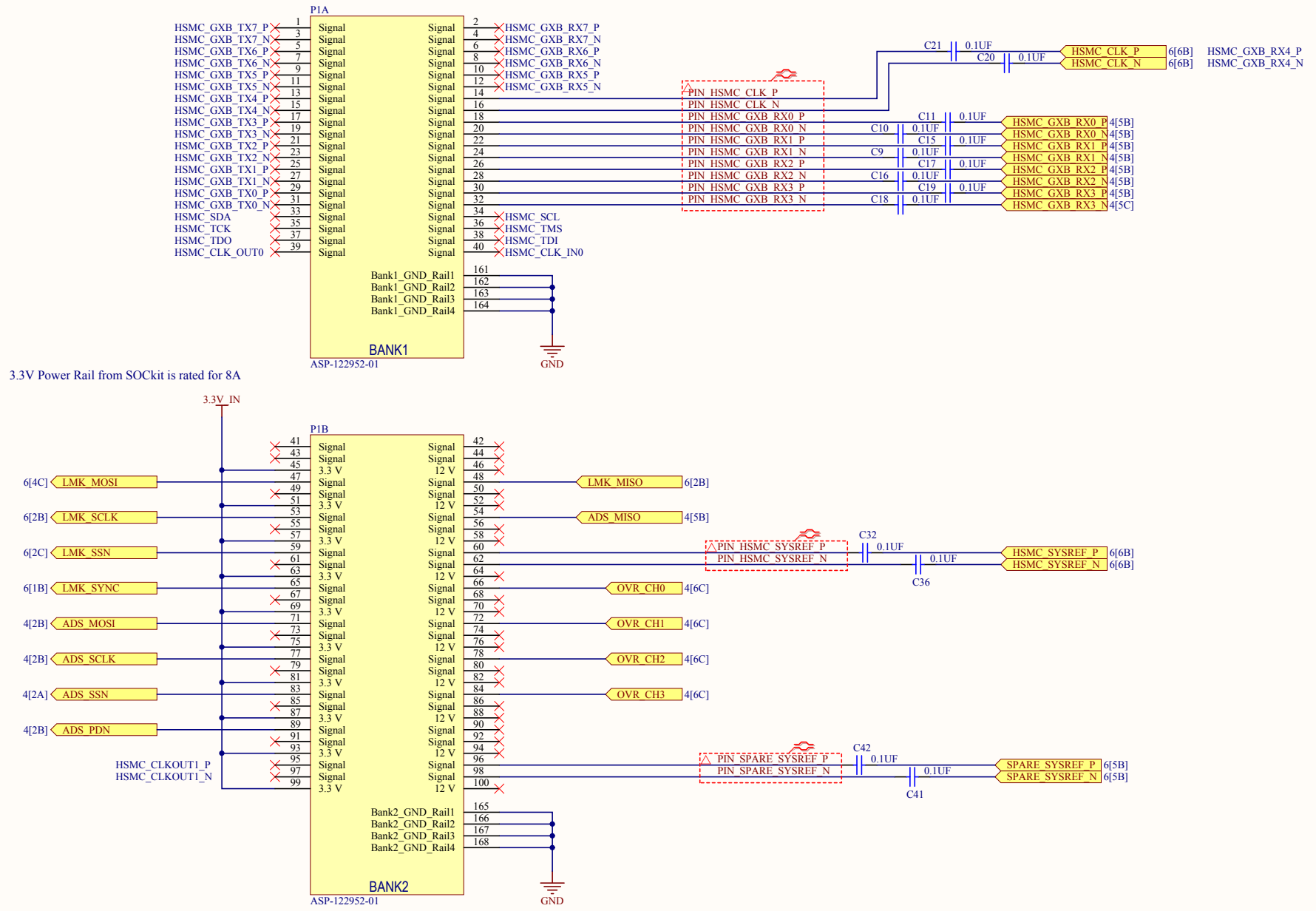
### REVISION TABLE

03-14-14	A	ET	Initial release of the schematic.
03-20-14	A1	ET	1.8V ADC power regulator biased to 1.86V output voltage.
06-02-14	B	ET	L18->1A device, F1-> 2A device, Set 240 Ohm R53 etc as DNP, Add 1UF to VCXO and OSC input filters, U2 VREG fix solder mask, change part numbers L13, L14, L15 for more current, change U8 ADC SYNC input termination to LVDS, LMK loop filter adjust.
07-03-14	B1	ET	All changes SH7, increase input BW from 80MHz to 200MHz. L1, L2, L3, L4 was 39nH, now 1.2nH. R7, R9, R16, R17 was 27.4 Ohm, now 59 Ohm. C14, C26 was 10pF, now DNP. C13, C27 was 10pF now 1.2pF.
08-17-14	B2	ET	Minor changes to schematic notes only.

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Title <b>HSMC, AD Converter, TI AD34JXX</b>		Dallas Logic Corporation 1512 Bray Central Drive Suite 115 Mckinney Tx 75069 USA		
Size: B	Number: DEV-ADC.	Revision: B2		
Date: 8/17/2014	Time: 1:19:00 PM	Sheet 1 of 9		
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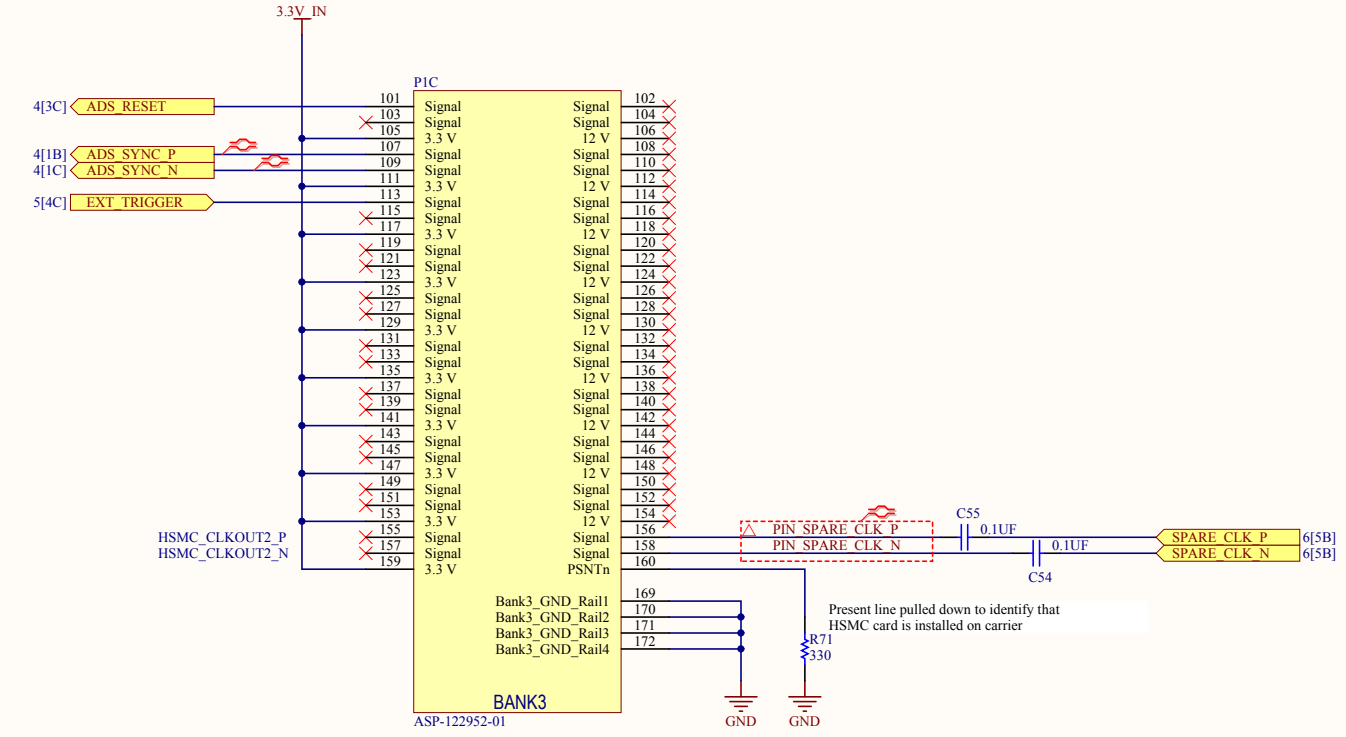
# HSMC CONNECTOR B1, B2




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# HSMC CONNECTOR B3

3.3V Power Rail from SOCKit is rated for 8A



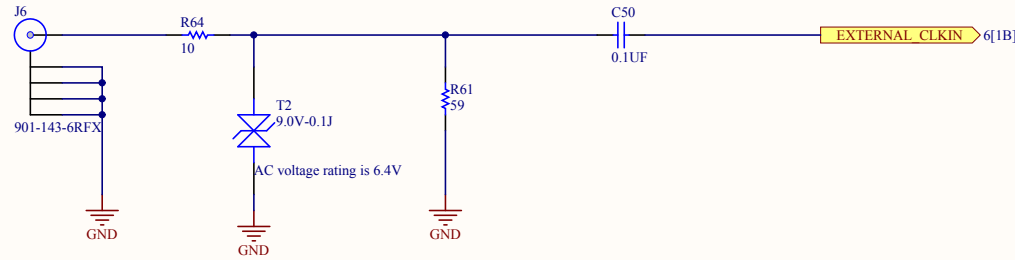
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Title <b>HSMC, AD Converter, TI AD34JXX</b>			Dallas Logic Corporation 1512 Bray Central Drive Suite 115 McKinney Tx 75069 USA 
Size: B	Number: DEV-ADC.	Revision: B2	
Date: 8/17/2014	Time: 1:19:01 PM	Sheet 3 of 9	
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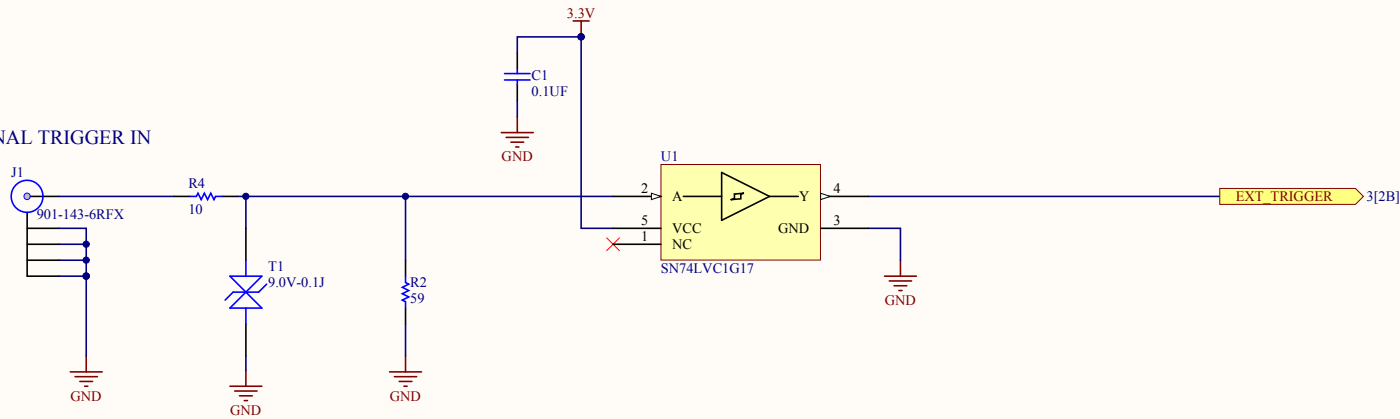


# CLOCK

EXTERNAL CLOCK IN



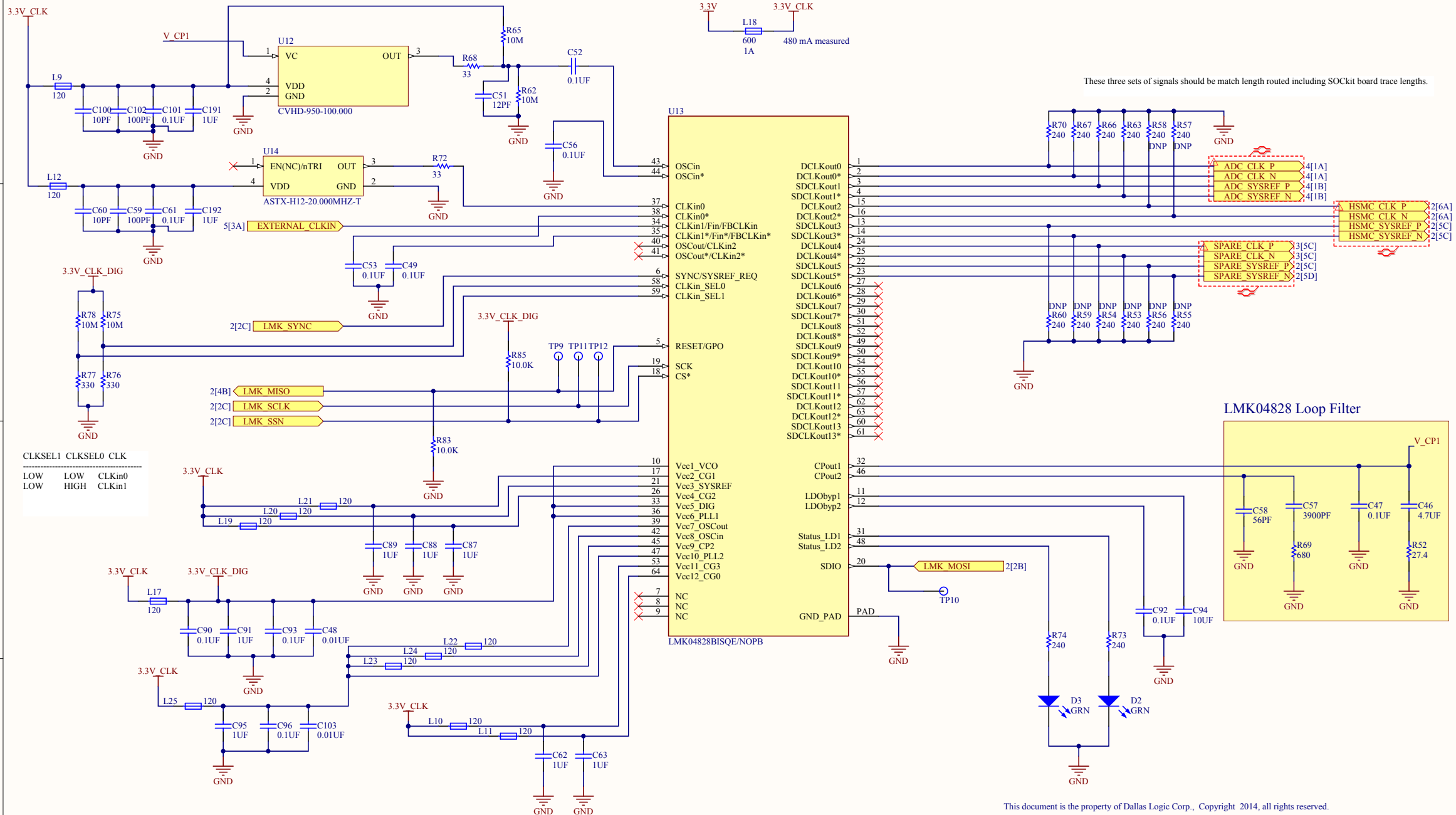
EXTERNAL TRIGGER IN



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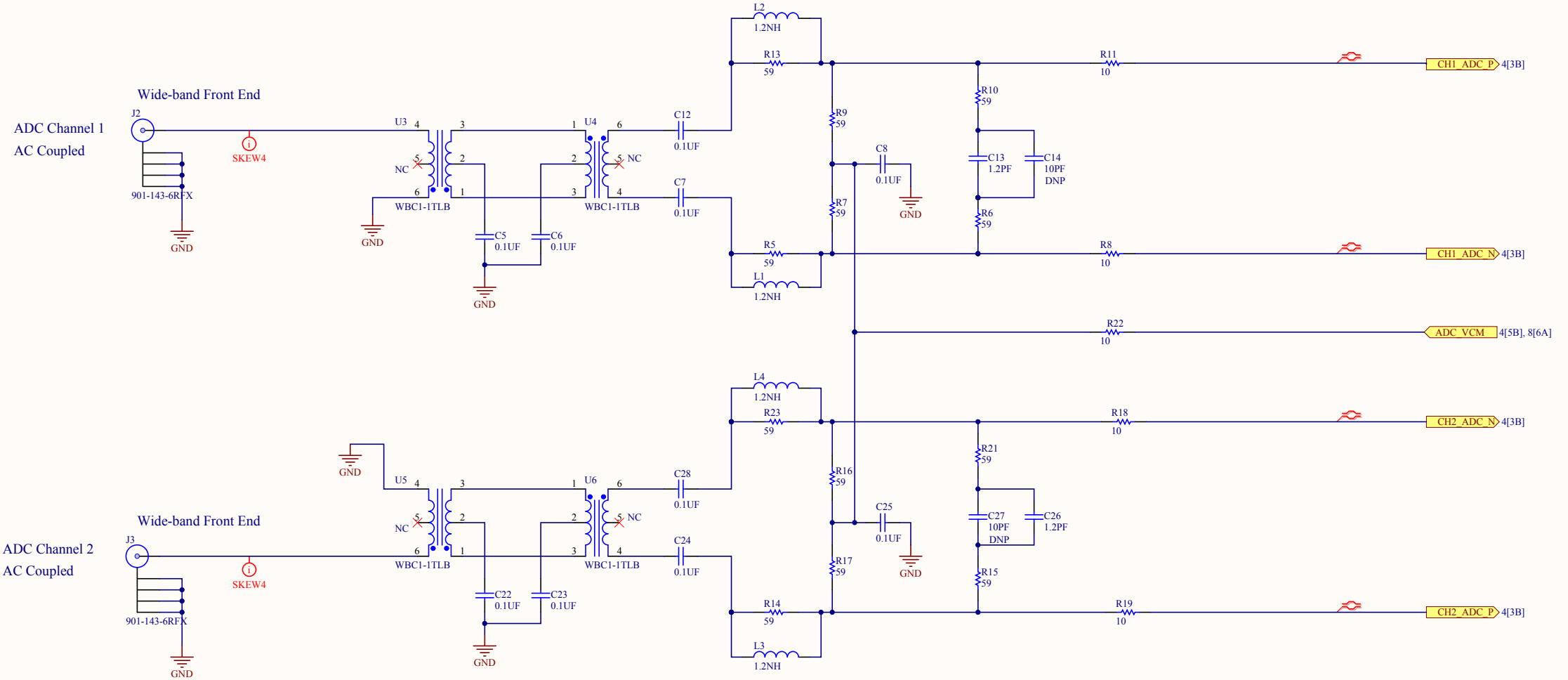
Title <b>HSMC, AD Converter, TI AD34JXX</b>		Dallas Logic Corporation 1512 Bray Central Drive Suite 115 McKinney Tx 75069 USA	
Size: B	Number: DEV-ADC.	Revision: B2	
Date: 8/17/2014	Time: 1:19:01 PM	Sheet 5 of 9	
File: C:\dallas_logic\altium_dlc\Projects\DEV-ADC34JXX_REV B5_CLK.SchDoc			

# CLOCK 2




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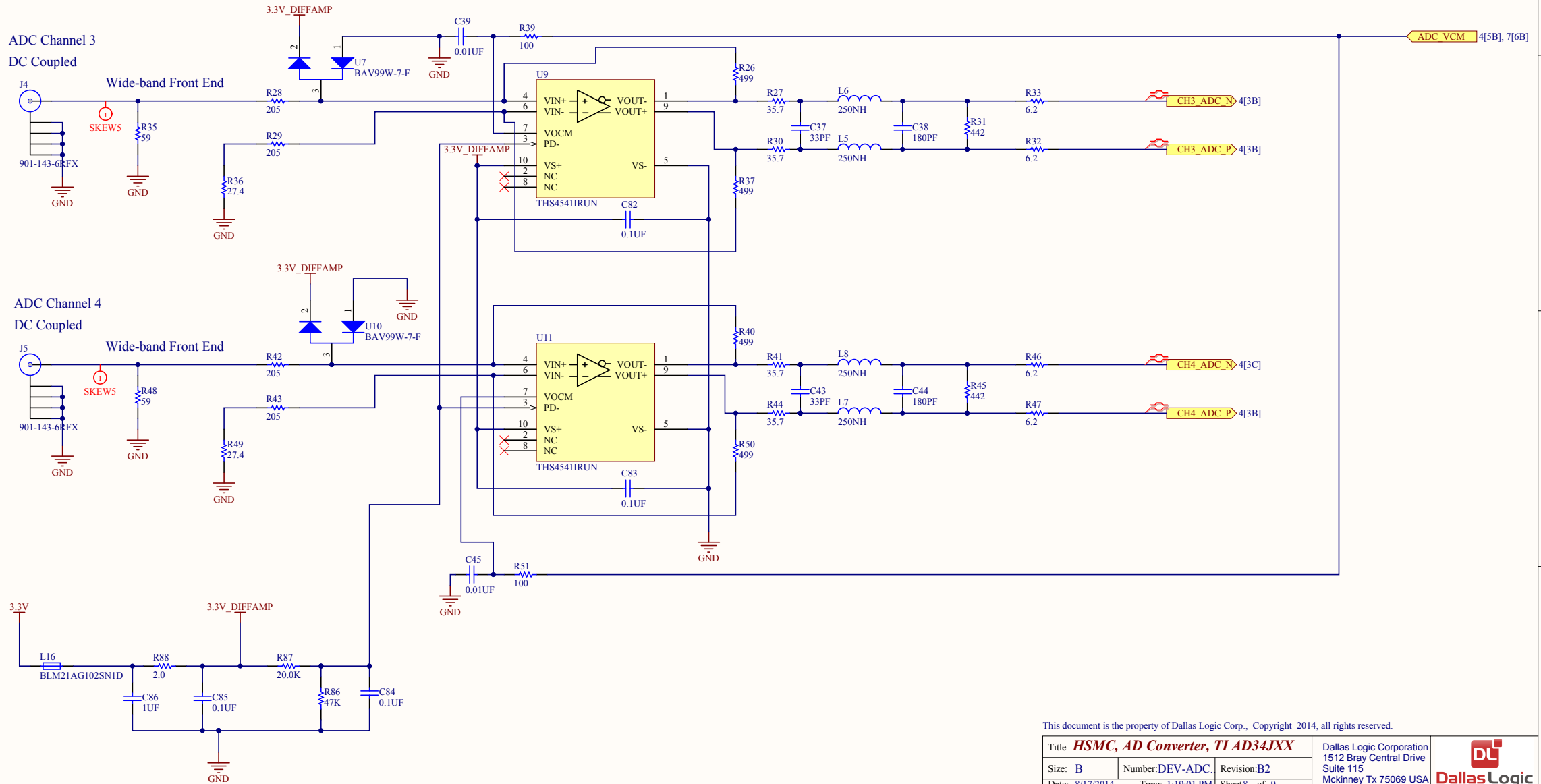
# FRONT END - AC COUPLED



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Size: B	Number: DEV-ADC. Revision: B2	
Date: 8/17/2014	Time: 1:19:01 PM Sheet 7 of 9	
File: C:\dallas_logic\altium_dlc\Projects\DEV-ADC34JXX_REV07_FE.SchDoc		

# FRONT END - DC COUPLED

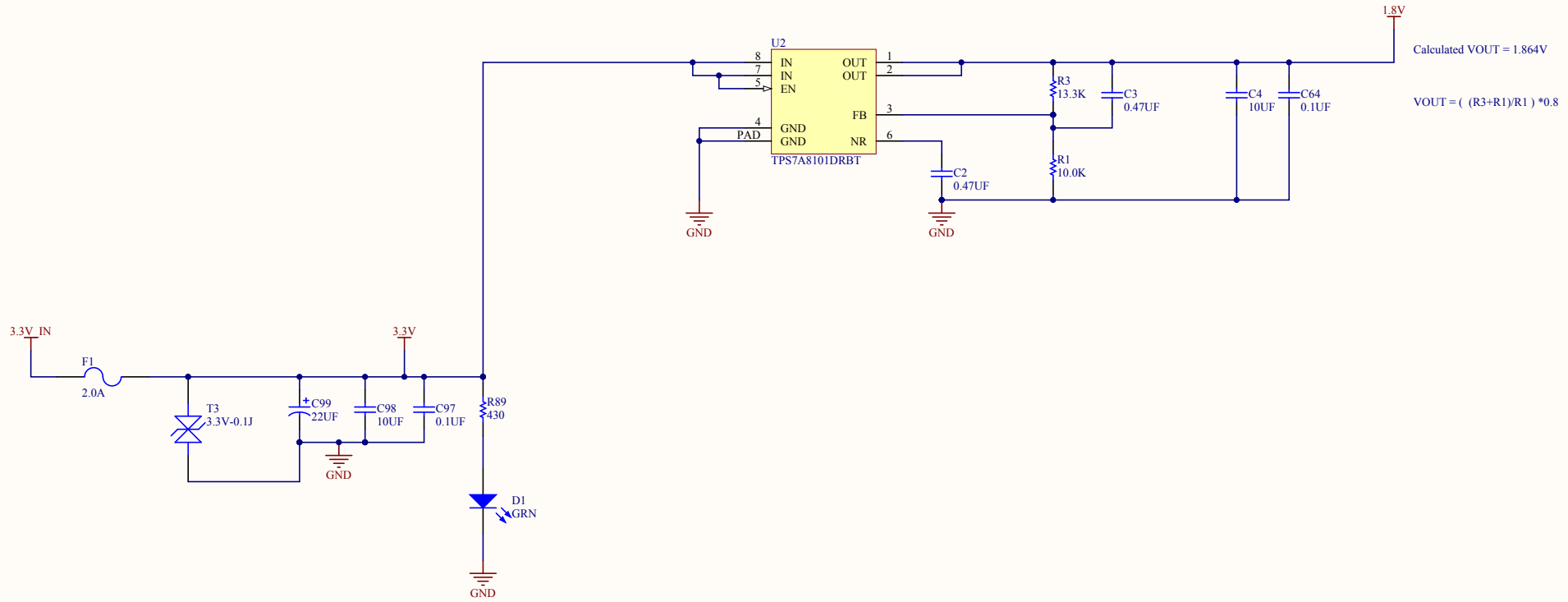


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Size: B	Number: DEV-ADC.	Revision: B2	
Date: 8/17/2014	Time: 1:19:01 PM	Sheet 8 of 9	File: C:\dallas_logic\altium_dlc\Projects\DEV-ADC34JXX_REV B8_FE2.SchDoc



# POWER SUPPLY



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Size: B	Number: DEV-ADC.	Revision: B2	
Date: 8/17/2014	Time: 1:19:01 PM	Sheet 9 of 9	File: C:\dallas logic\altium dlc\Projects\DEV-ADC34JXX REVB9 PWR.SchDoc