ADC 34J22 HIGH SPEED MEZZANINE CARD (HSMC)

DEV-ADC34J22 User Guide

1512 Bray Central Drive #115
McKinney, TX 75069
www.dallaslogic.com

Version 1.0- July 2014

Table of Revisions

Revision	Author	Date	Description
1.0	JT	08-04-2014	Released

Table of Contents

List of Figures

List of Tables

1 Introduction

The DEV-ADC34J22 is a four channel ADC daughter card which features Texas Instruments ADC34J22. The 34J22 is a quad, 12 bit, 50Msps, JESD204B compliant analog to digital converter. In addition to the 34J22, the design includes Texas Instruments LMK04828B. The LMK04828B is a JESD204B compliant clock jitter cleaner with dual loop PLL devices. This development board has a HSMC connector and is compatible with Altera's HSMC (High Speed Mezzanine Card) module specification [1]. The module can be clocked using an on-board 10 MHz. TCXO or can be supplied an external input clock via a front panel SMA. An external trigger input is provided for custom sampling control. The ADC channels are organized into two groups designed to support different applications. ADC Channels 1 & 2 are transformer coupled and support operating frequencies from 200 kHz to 200 MHz. ADC channels 3 & 4 are DC coupled using a differential amplifier and support operating frequencies from 0 Hz to 20 MHz.

Below is a summary of the DEV-ADC34J22's feature set:

- Texas instruments ADC34J22, four channels, 12bit, 50 MSPS, JESD204B compliant analog to digital converter.
- Four, SMA input signal connectors.
  - Channels 1 & 2 include a transformer coupled front end.
  - Channels 3 & 4 include a differential amplifier front end.
- One, SMA input clock connector
- One, SMA Trigger Input connector.
- On board 10 MHz TCXO.
- On module TI LMK04828B Dual Loop Clock Jitter Cleaner
- HSMC connector for interfacing with a FPGA based carrier module.
- SPI control interfaces for both the ADC and LMK devices

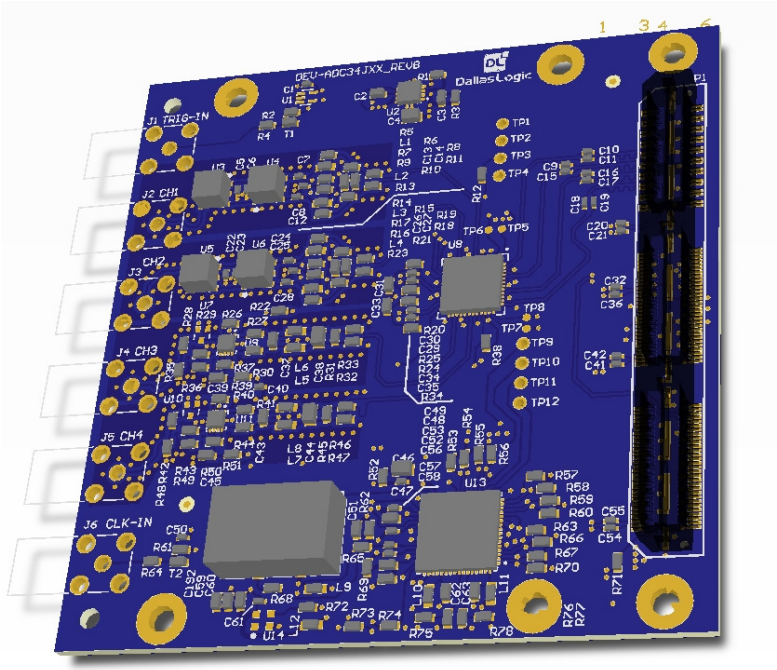

Figure 1-1 DEV-ADC34J22 Module Rendering

The following figure identifies the major functional blocks found on the DEV-ADC34J22.

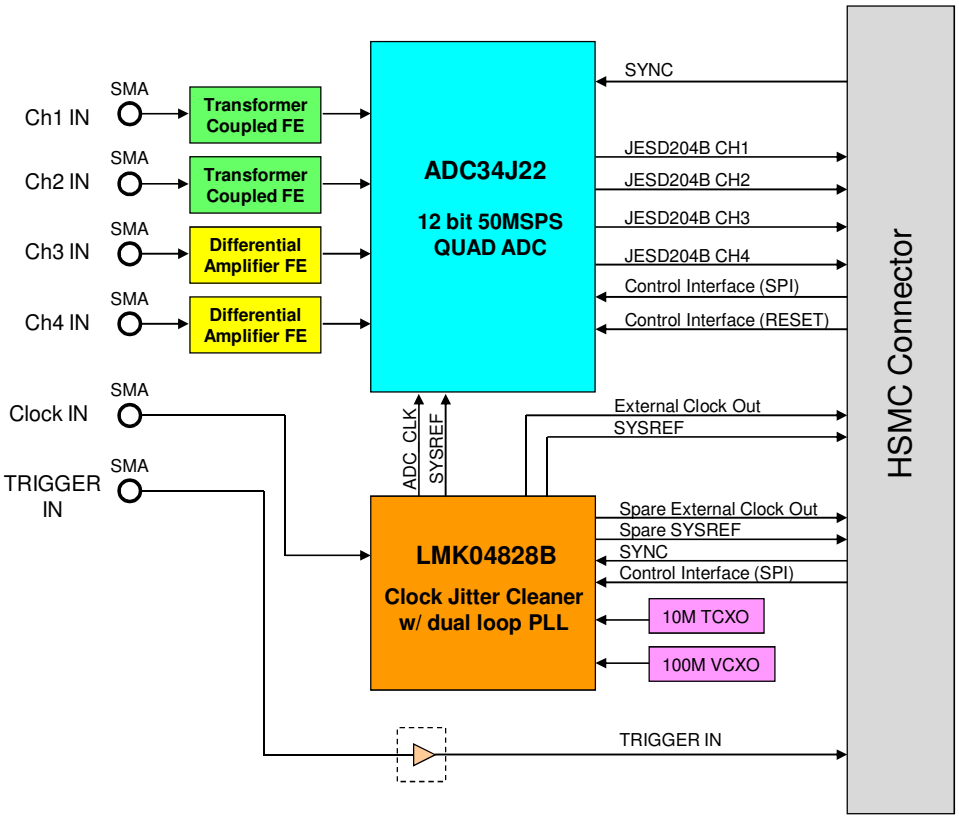

Figure 1-2 DEV-ADC34J22 Block Diagram

2 Analog Section

2.1 Front End

The DEV-ADC34J22 module supports four analog inputs. Two inputs are DC coupled and two inputs are AC coupled.

Table 2-1 DC Coupled Front End Input Specifications

Category	Specification
Number of Analog Channels	2
Input Range	+/- 0.5V (1 V p-p)
Input Bandwidth	DC – 15 MHz
Input Impedance	50 ohms

Table 2-2 AC Coupled RF Front End Input Specifications

Category	Specification
Number of Analog Channels	2
Full Scale Input Voltage	+/- 1.0V (2 V p-p)
Input Bandwidth	0.1 – 200 MHz
Input Impedance	50 ohms

2.1.1 Transformer coupled inputs

Channels 1 & 2 are designed to support low IF based sampling for frequencies up to 200 MHz. This bandwidth supports operation in Nyquist zones 1 through 8 when operating at a 50 MHz sample rate. The transformer coupled channels each utilize a pair of back to back transformer arranged with opposite polarity to minimize the effects of phase imbalance between the positive and negative differential signals. This dramatically improves the harmonic performance of the ADC resulting in excellent Spurious Free Dynamic Range (SFDR) performance.

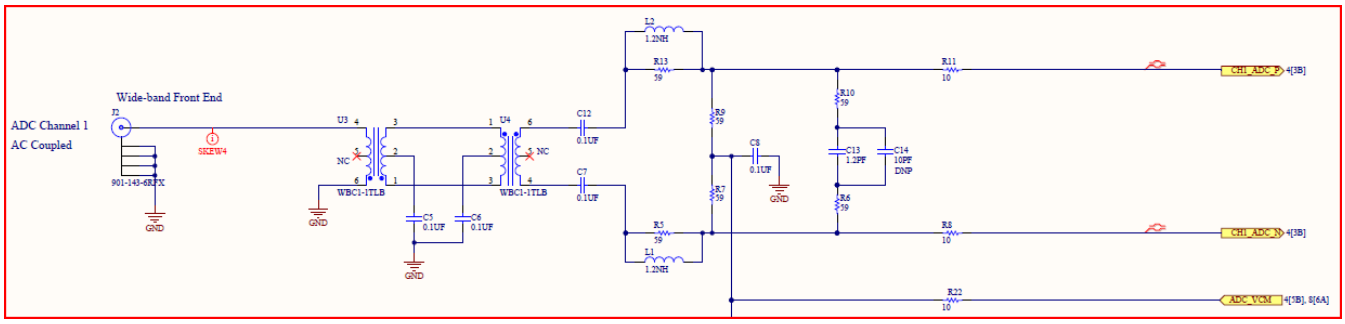

Figure 2-1 Transformer Coupled Analog Input Schematic Diagram

The frequency response of the transformer coupled channel is driven by the filter following the transformers. The WBC1-1TLB transformers have a frequency response to greater than 700 MHz. The filter provides a cutoff frequency of about 200 MHz as shown in the following plot of the frequency response.

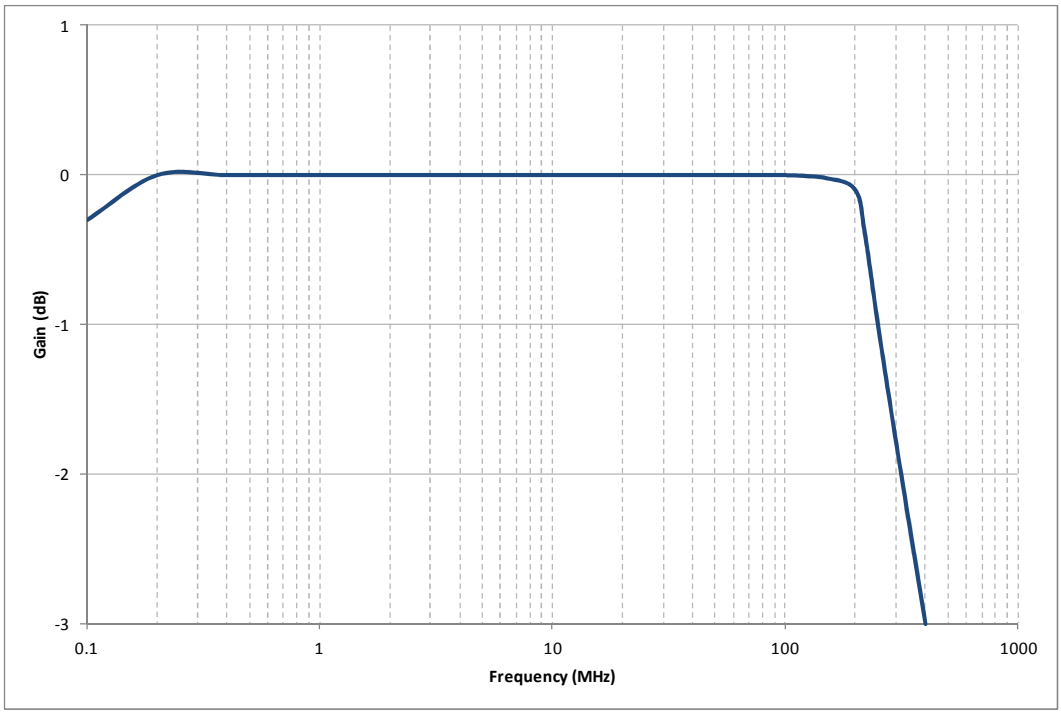

Figure 2-2 Transformer Coupled Channel Frequency Response

2.1.2 DC Coupled Inputs

Channels 3 & 4 are designed to support low frequency and zero IF based sampling for frequencies up to 20 MHz. This bandwidth only supports operation in the first Nyquist zone. The DC coupled channels each utilize a Texas Instruments THS4541 high performance fully differential amplifier to transform the single ended input signal to a differential signal suitable for the ADC IC input. This device provides a gain of 2 V/V (6 dB). The use of the THS4541 maintains excellent harmonic performance for and active channel resulting in great Spurious Free Dynamic Range (SFDR) performance.

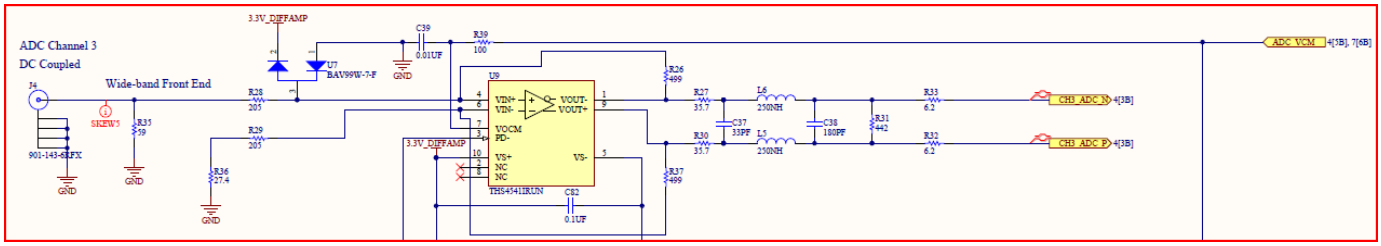

Figure 2-3 DC Coupled Analog Input Schematic Diagram

The frequency response of the DC coupled channels is driven by filter following the differential amplifier. The THS4541 has a frequency response of greater than 700 MHz with a gain of 2 V/V. The filter provides a cutoff frequency of about 20 MHz as shown in the following plot of the frequency response.

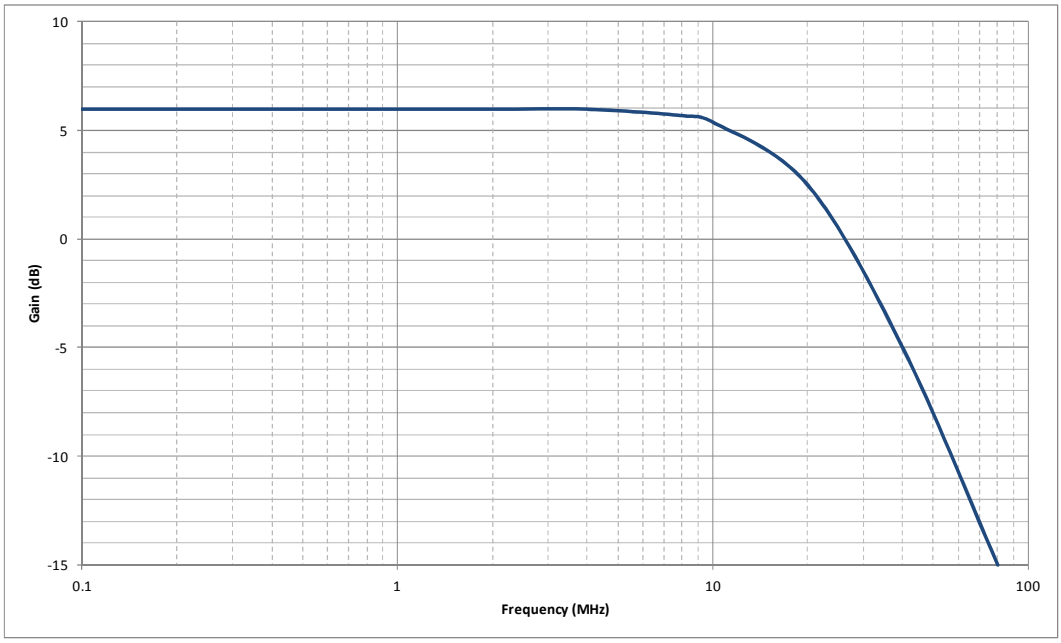

Figure 2-4 DC Coupled Analog Input Schematic Diagram

2.1.3 Channel Performance

The following figures provide an example of the SNR and SFDR performance achieved using this module. A 4.98046875 MHz. sinusoid was input on each of the four channels and the results were analyzed using Texas Instrument's High Speed Data Converter Pro V 2.50 signal analysis tool.

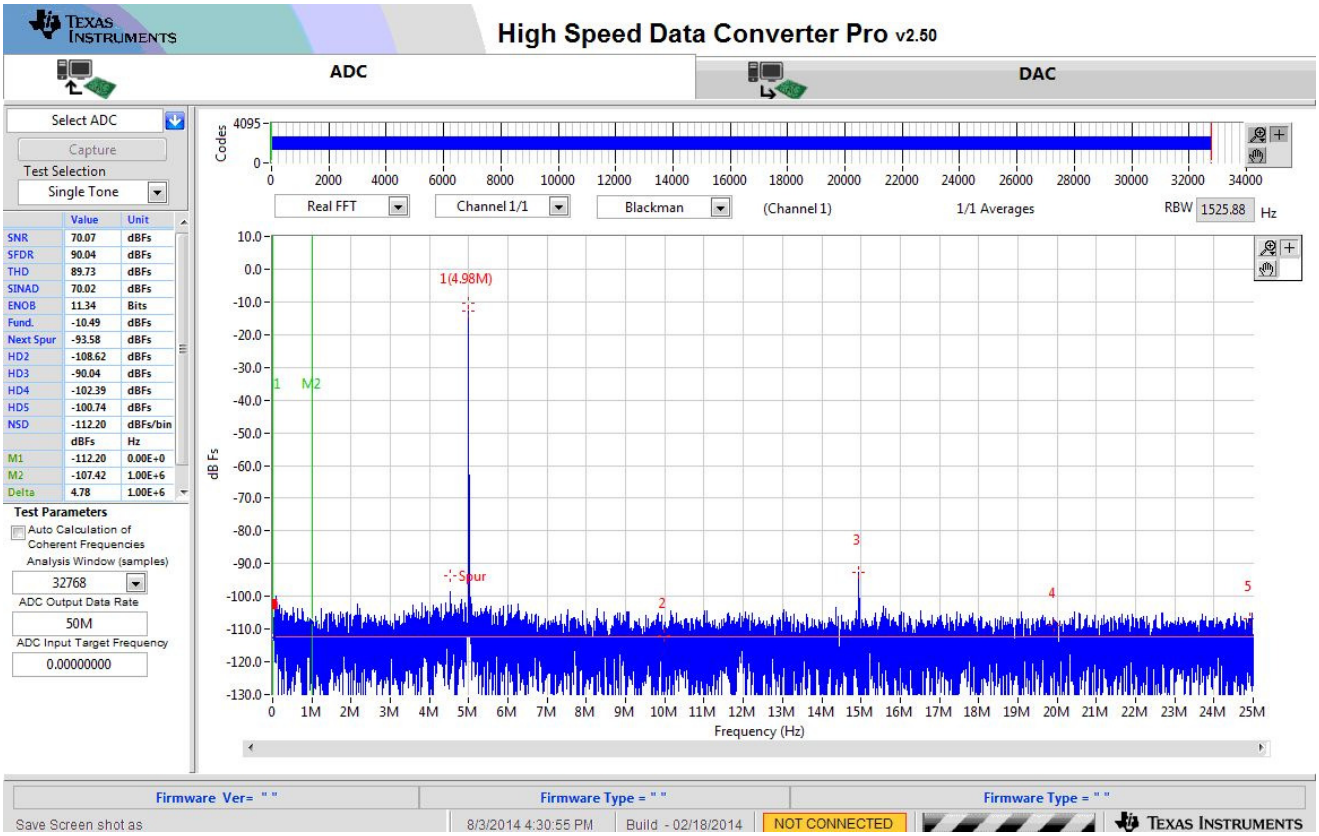

Figure 2-5 Channel 1 Performance

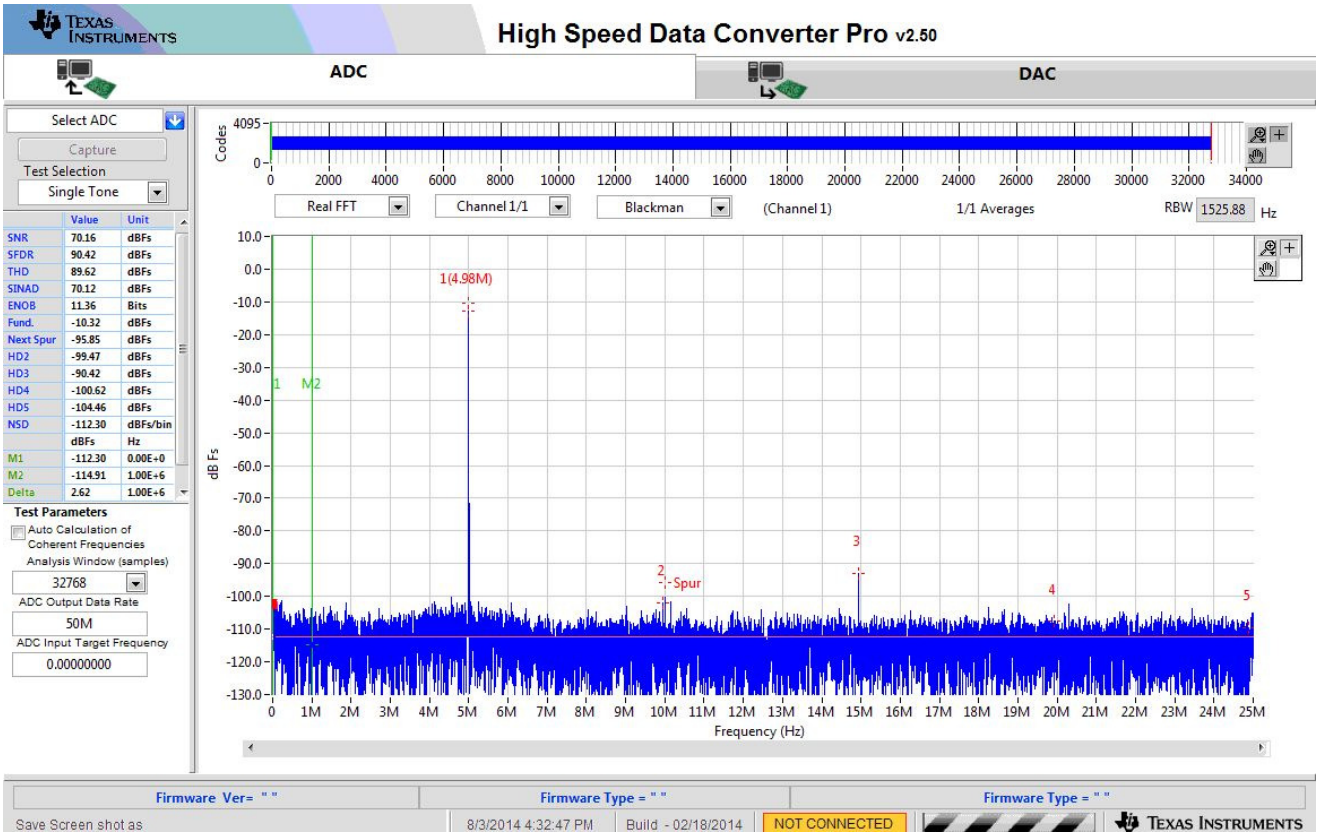

Figure 2-6 Channel 2 Performance

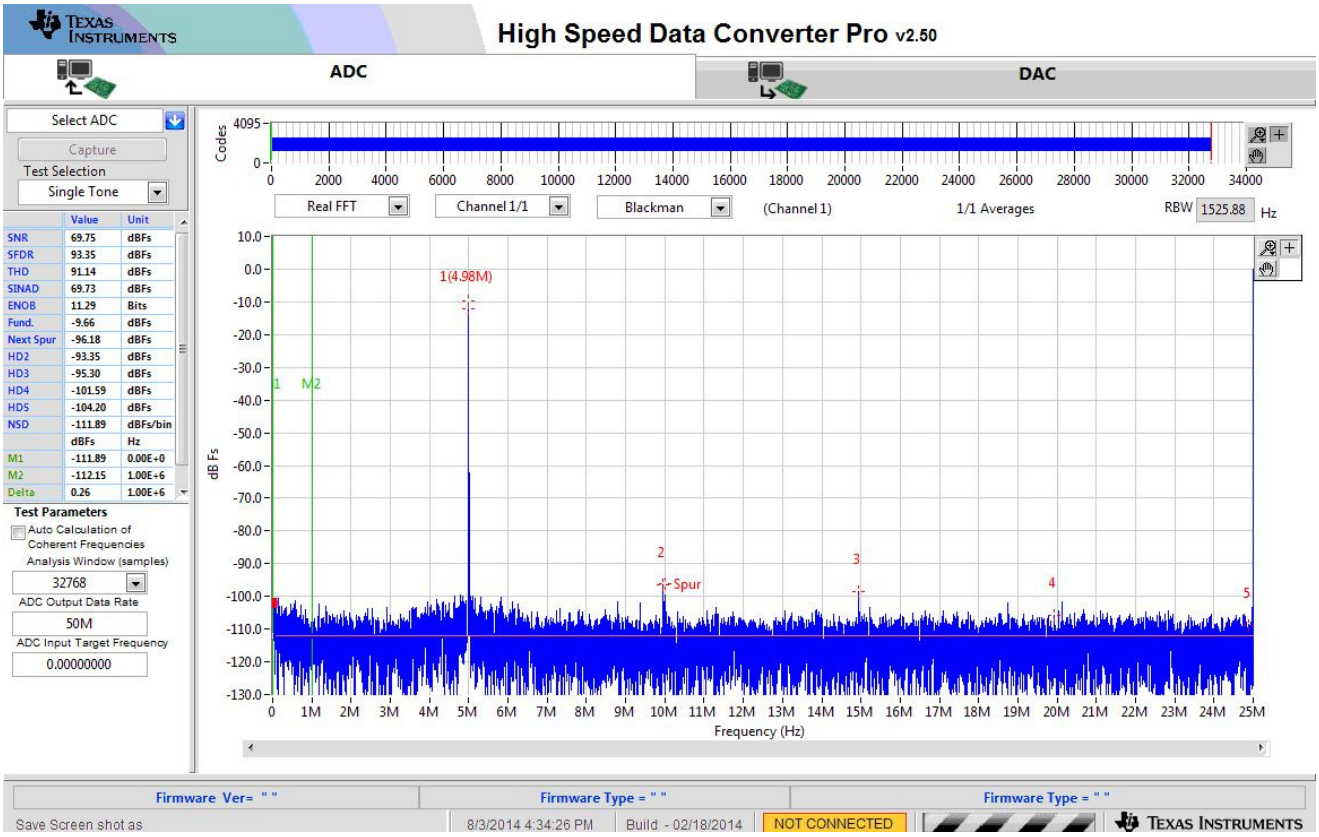

Figure 2-7 Channel 3 Performance

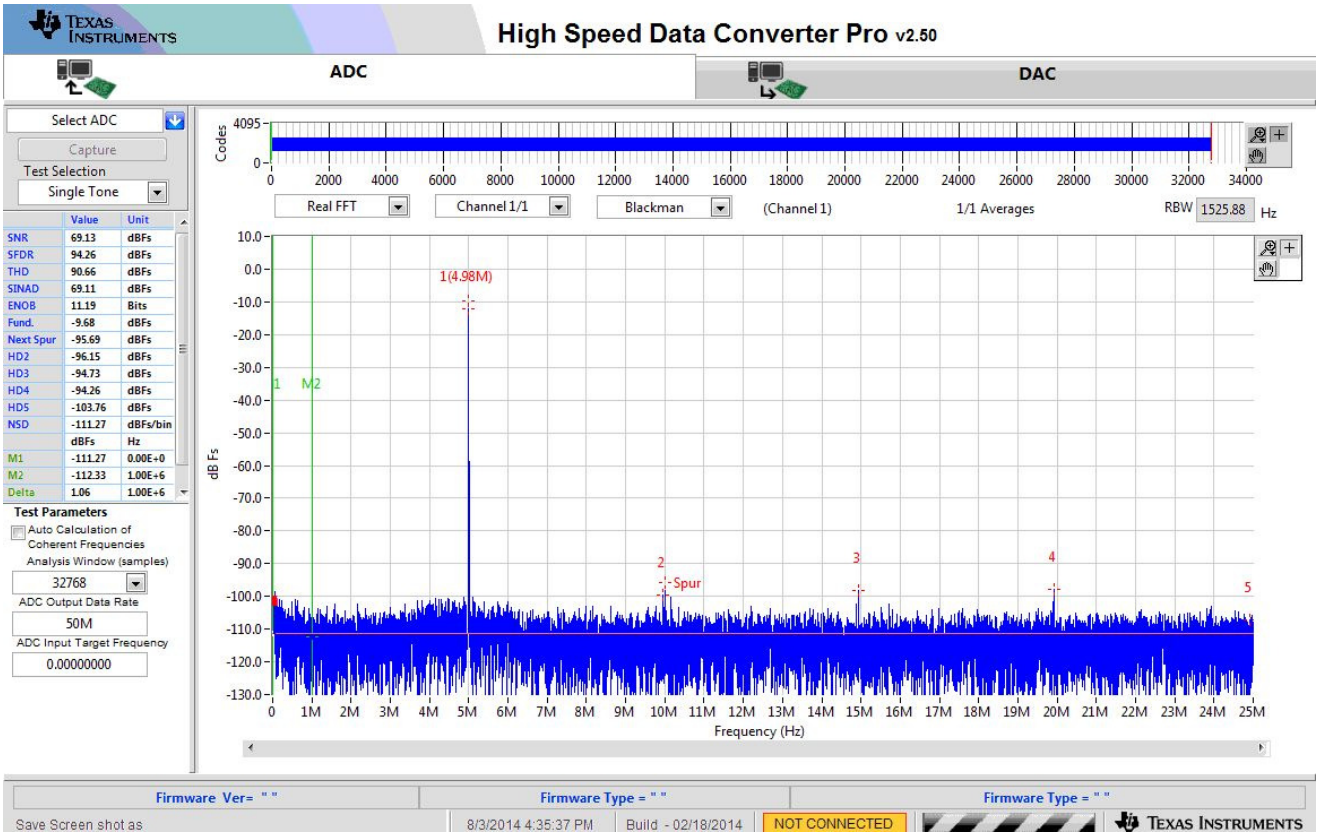

Figure 2-8 Channel 4 Performance

2.2 Analog to Digital Converter

The DEV-ADC34J22 HSMC module implements the Texas Instrument's ADC34J22 Analog to Digital Converter. The ADC34J22 is a quad channel device with a JESD204B digital interface. The ADC has the following performance specifications.

Table 2-3 Analog to Digital Converter Specifications

Category	Specification
Sample Rate	≤ 50 MSPS
SNR minimum (Dither On) • 10 MHz • 70 MHz • 100 MHz • 170 MHz • 230 MHz	 70.6 dBFS 70.1 dBFS 70.2 dBFS 68.9 dBFS 67.9 dBFS
SFDR minimum (Dither On) • 10 MHz • 70 MHz	 100 dBc 92 dBc

• 100 MHz • 170 MHz • 230 MHz	88 dBc 85 dBc 79 dBc
Non HD2,3 (Dither On) • 10 MHz • 70 MHz • 100 MHz • 170 MHz • 230 MHz	 95 dBc 95 dBc 96 dBc 96 dBc 94 dBc

The ADC device is configured via a SPI interface sourced from the host HSMC carrier. The default configuration file for the ADC device is located in appendix A of this document.

3 Clock & Synchronization Specifications

The diagram below shows the clock and synchronization interfaces on the DEV-ADC34J22 module. These interfaces are implemented to support the JESD204B (sub class 1) protocol interface that is used for data transmission between the FPGA and the ADC34J22.

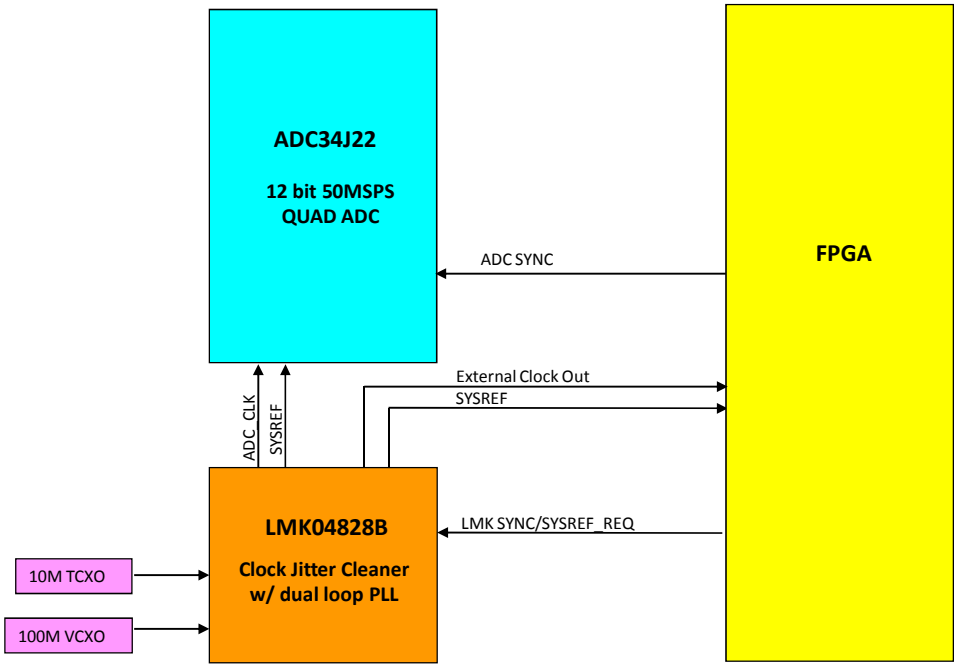

Figure 3-1 Clock and Synchronization Interface Diagram

In diagram above the LMK04828B is used to generate the Device Clock and SYSREF to both the JESD204B core operating in the FPGA as well as the ADC34J22. Immediately following power-up the FPGA's JESD204B core will send a SYNC/SYSREF_REQ request to the LMK and ADC, upon receiving this request the ADC will begin it's lane synchronization procedures, these include CGS (Code group Synchronization) and ILA (Initial Lane Alignment).

The LMK upon receiving the SYNC/SYSREF_REQ signal will begin transmitting the SYSREF signal. This is a low frequency synchronization clock that is used to synchronize the LMFC (Local multi-frame clock) operating in both the FPGA and ADC. Please refer to the device datasheets for additional information about the JESD204B interface.

3.1 On Board Reference Clock

The primary/default reference clock for the DEV-ADC34J22 HSMC module is an onboard TCXO. This allows the operation of the ADC module without an external clock source. The onboard clock provides the reference signal for the first loop of the LMK04828B jitter cleaner. The TCXO has the following specifications.

Table 3-1 Onboard Clock Specifications

Category	Specification
Output Standard	3.3V (HCMOS)
Onboard Clock Frequency	10 MHz
Phase Noise (Frequency Dependant)	-130 dBC (@ 1kHz offset)
	-158 dBC (@100kHz offset)

3.2 Reference Clock Selection

The DEV-ADC34J22 HSMC module may optionally be configured to use either an external reference clock or the onboard TCXO. The onboard TCXO is the default selection for the reference. The external clock input is available via a SMA connector (J6) located on the front of the module. The clock input has the following specifications.

Table 3-2 Clock Input Specifications

Category	Specification
Number of Clock Inputs	1
Input Clock Frequency	10 - 160 MHz
Duty Cycle	40% to 60%
Input Voltage	Single ended, AC / DC coupled (MOS, .35 – 2.4 Vpp) (Bipolar, .25 – 2.4 Vpp)
Input Impedance	50 ohms

When selecting the external clock input, a modification to the module is required. Clock selection is made using 4 strapping resistors. The following table identifies the supported clock input configurations. Note that the clock input selection is made by the LMK04848B device based on the CLKSEL0 and CLKSEL1 inputs.

Table 3-3 Clock Selection

Clock Source	CLKSEL1	CLKSEL0	Loaded Resistor Value			
			R78	R75	R77	R76
CLKin0 (onboard TCXO)	LOW	LOW	10M	10M	330	330
CLKin1 (External Clock)	LOW	High	10M	1K	330	10M

3.3 Jitter Cleaner

The onboard LMK04828B is a low noise, clock jitter cleaner with dual loop PLLs. The device is JESD204B compliant and supports all of the JESD specifications clocking modes including subclass 0, 1 and 2. The DEV-ADC34J22 HSMC default configuration is based on the 10 MHz reference clock TCXO and a 100 MHz ultra low noise VCXO as the VCO for the first PLL loop. The LMK04828B internal VCO is used as the VCO for the second loop. The default configuration creates a final ADC clock frequency of 50 MHz. The loop 1 VCXO and the loop 2 VCO specifications are shown in the following tables.

Table 3-4 Loop 1 VCXO

Category	Specification
Output Standard	3.3V (HCMOS)
VCXO Frequency	100 MHz
Control Voltage	1.65V ±1.65V
Tuning Sensitivity	+25 ppm/V Typical
Phase Noise (Frequency Dependant)	-143 dBC (@ 1kHz offset)
	-157 dBC (@ 10kHz offset)
	-164 dBC (@100kHz offset)

Table 3-5 LMK04828B internal VCO ranges

VCO 0	VCO 1
2370 to 2630 MHz.	2920 to 3080 MHz.

The LMK device is configured via a SPI interface sourced from the host HSMC carrier. The default configuration file for the LMK device is located in appendix B of this document.

3.4 Trigger Input

An external trigger is available on the HSMC module via the (J1) SMA connector. The trigger input is buffered on the HSMC module and then routed to the HSMC connector.

Table 3-6 Synchronization I/O Specifications

Category	Specification
Number of Synch Inputs	1
Voltage	Single ended LVCMOS
Impedance	50 ohms

4 Digital Specifications

4.1 JESD204B Interface

4.1.1 Data Interface

The DEV-ADC34J22 Digital interface supports sub-class 0 and sub-class 1 of the JEDEC, JESD204B standard. The module is organized to use four lanes operating at a maximum frequency of 3.2 Gbps. All of the signals are AC coupled to the HSMC connector.

Table 4-1 JESD204B Output Specifications (DxP, DxM)

Parameter	Comments	Min	Typ	Max	Unit
High-level output voltage			1.8		V
Low-level output voltage			1.4		V
Output differential voltage			400		mV
Output offset voltage	Common-mode voltage of OUTP and OUTM		1.6		V

4.2 Configuration

The DEV-ADC34J22 module has two configurable devices, the ADC34J22 and the LMK04828B. Both of these devices are configurable via independent SPI interfaces.

4.2.1 ADC Serial control interface

The ADC's serial interface includes the following signals, PDN, SEN, SCLK, SDATA, and SDOUT. The interface is driven from the HSMC connector.

Table 4-2 ADC34J22 Control Interface Signals

SIGNAL	Description	Voltage Level
PDN	Power Down Control	1.8V (active low signal)
SEN	Serial Interface Enable	1.8V (active low signal)

SCLK	Serial Interface Clock Input	1.8V
SDATA	Serial Interface Data Input	1.8V
SDOUT	Serial Interface Data output	1.8V
RESET	Hardware Reset	1.8V (active high signal)

4.2.2 LMK04828B Serial control interface

The LMK's serial interface includes the following signals, RESET/SDO, CSN, SCK, and SDIO. The interface is driven from the HSMC connector.

Table 4-3 LMK04828B Control Interface Signals

SIGNAL	Description	Voltage Level
CSN	Serial Interface Enable	3.3V (active low signal)
SCK	Serial Interface Clock Input	3.3V
SDIO	Serial Interface Data Input	3.3V
RESET/SDO	Serial Interface Data output. (This is a multi-function signal which can also be configured as RESET)	3.3V

The DEV-ADC34J22 module uses the LMK04828B's RESET/GPO signal as a serial data out signal. Thus in order to issue a reset to the device, bit 7 of Register address 0x000 should be used.

4.3 Arrow SOCkit Board Support

The DEV-ADC34J22 was designed to interface with Arrow's SOCkit evaluation board. The SOCkit features Altera's 5CSXFC6D6F31C7 SOC FPGA. The design integrates MTI's JESD204B IP core and utilizes the onboard dual ARM9 core for configuring the DEV-ADC34J22 module. Additional information can be downloaded from Arrow's DEV-ADC34J22 information page located here:

http://arw.ae/devadc34j22

4.3.1 MTI IPC-JESD204-B TX/RX IP core

The reference design includes an evaluation version of the MTI JESD204-B RX IP core. A license is required to use the reference design. For additional information about obtaining a evaluation license please use Altera's JESD204B Resource Center located at this website:

http://www.altera.com/technology/high_speed/protocols/jesd204b/je-index.html?utm_source=altera&utm_medium=homepage_ad&utm_campaign=jesd204b/

5 Power

5.1 Voltage and Current Requirements

The DEV-ADC34J22 uses the 3.3V power rail provided by the HSMC carrier (+3.3V input via the HSMC connector). The power input is protected with a 2 Ampere fuse. Typical overall current draw at 3.3V is xx.xx mA. The table below provides more detail on the module power based on specific device.

Table 5-1 HSMC Voltage and Current By Device

Carrier Voltage Supply	Voltage Level	HSMC Function	Current Requirement
3P3V	3.3V	Differential Amplifier	150mA
		10MHz. TCXO	4.8mA
		100MHz. VCXO	15mA
		TI LMK04828B	370mA (3 outputs selected)
	1.8V	ADC34J22	272mA (4 channels)

5.2 Power Dissipation

The following table identifies the primary components and their typical power consumption.

Table 5-2 HSMC Power By Device

Voltage Rail	Module Function	Current Requirement	Power
3.3V	Differential Amplifier	150mA	495 mW
	20MHz. TCXO	4.8mA	15.84 mW
	100MHz. VCXO	15mA	49.5 mW
	TI LMK04828B	370mA (3 outputs selected)	1221 mW
1.8V	ADC34J22	272mA (4 channels)	489.6 mW
		Total Power	2270.94 mW

6 Mechanical and Environmental

6.1 Mechanical

The DEV-ADC34J22 module is based on Altera's High Speed Mezzanine Card (HSMC) specification. This specification provides an electromechanical architecture for quickly connecting IO systems to FPGA based carrier host boards. The HSMC specification fixes the width (Y dimension shown below, with connector) at 3.076 in. The length (X dimension shown below) for the DEV-ADC34J22 module is 3.0 in. There is 5mm of space between the carrier and host board. The mounting holes are 0.125 in. diameter and are plated with a 0.250 in. pad size. The holes are not connected to HSMC ground or shield. The HSMC module PCB thickness is 0.063 in. (1.6 mm). Note that there is an extra pair of 0.125 in. holes at the SMA end of the HSMC module. This allows a stable and vibration resistant installation of the DEV-ADC34J22 to a host board for various applications.

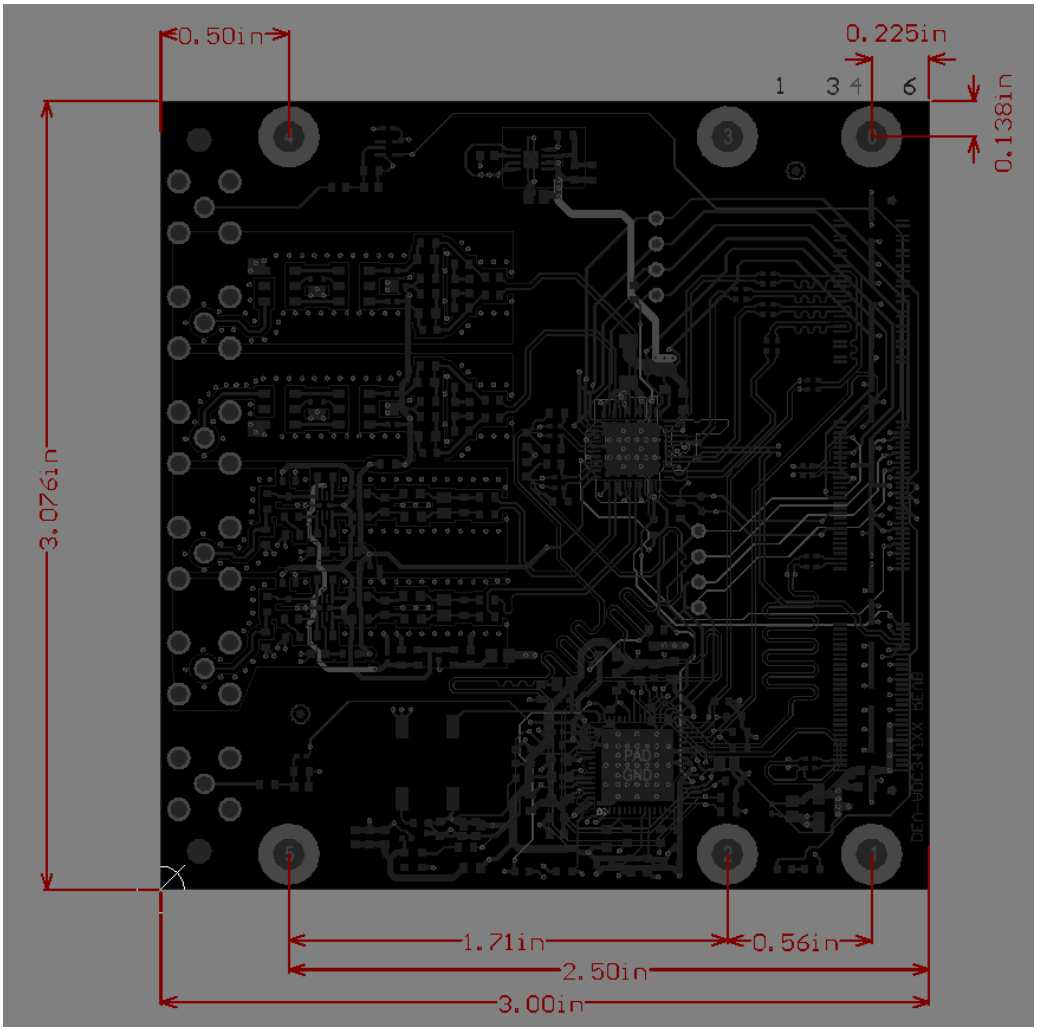

Figure 6-1 DEV-ADC34J22 Module Mechanical Dimensions

The majority of IC devices and components for the DEV-ADC34J22 are mounted on the same PCB side as the Samtec HSMC connector. For the SOCKIT carrier application, the DEV-ADC34J22 hangs off the edge of the host SOCKIT board (away from SOCKIT). Therefore, there is no interference between components on the Host

carrier or HSMC module. If an application requires the DEV-ADC34J22 to be mounted over a (different) host carrier board, attention must be paid to the location of DEV-ADC34J22 components to insure that there is no component interference (carrier to module).

The following diagrams are re-printed here for convenience from Altera's HSMC specification. These diagrams show the dimensions for an HSMC module (mezzanine card).

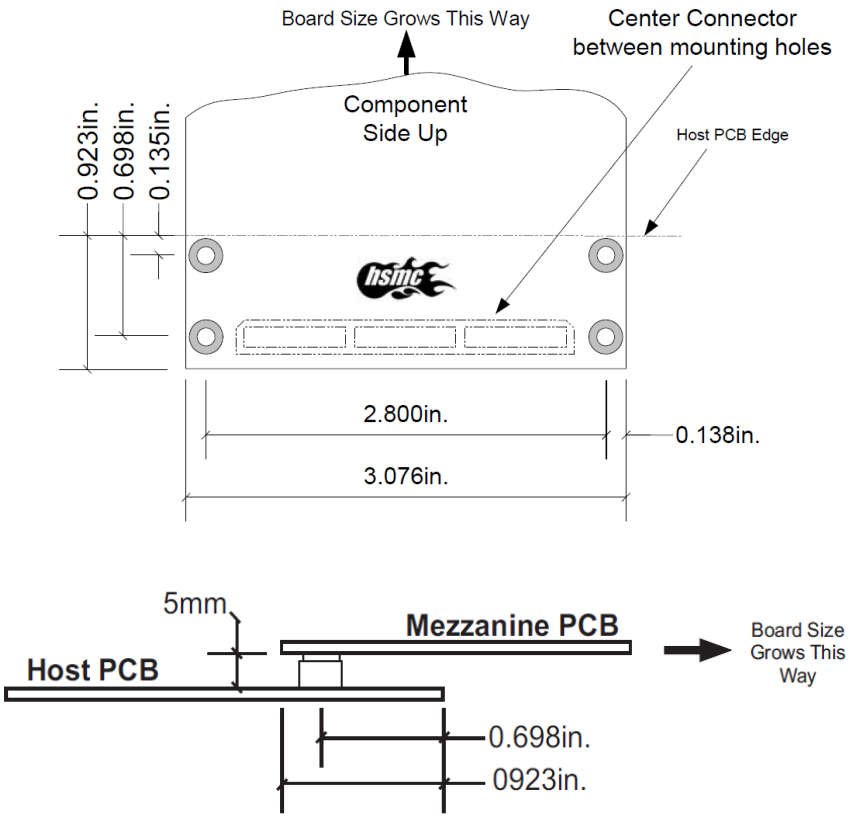

Figure 6-2 HSMC Specification Module Dimension Diagrams

6.2 HSMC connector

The DEV-ADC34J22 uses the Samtec ASP-122952-01 HSMC Connector (mezzanine card connector). The host -board will utilize the ASP-122953-01 (HSMC Host Board Connector). The following diagrams are re-printed here for convenience, from Altera's HSMC specification.

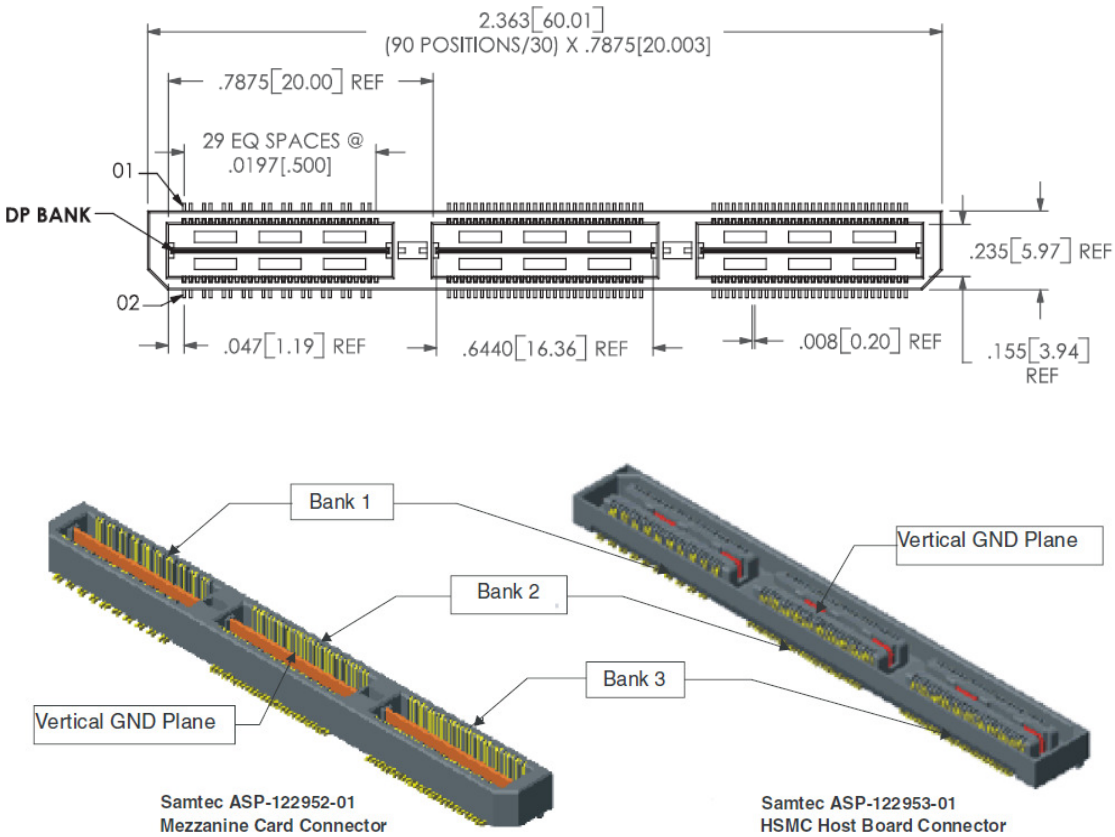

Figure 6-3 HSMC Specification Connector Diagrams

6.3 Environmental

The DEV-ADC34J22 HSMC is designed with commercial grade components, and is designed to operate over a temperature range of 0°C to 70°C.

7 References

1. HSMC Specification, Altera Corporation, June 2009.
2. SBAS669, ADS34J22 Datasheet, Texas Instruments, May 2014.
3. SNAS605 AP, LMK0482XB Datasheet, Texas instruments, March 2013.

8 Appendix A – ADC34J22 Configuration

```
static const DEVICE_DATA defaultData [NUM_REGISTERS] =
{
    { 0x00, 0x00},
    { 0x01, 0xff},
    { 0x02, 0x00},
    { 0x03, 0x00},
    { 0x04, 0x00},
    { 0x05, 0x00},
    { 0x06, 0x04},
    { 0x07, 0x04},
    { 0x08, 0x04},
    { 0x09, 0x06},
    { 0x0a, 0x00},
    { 0x0b, 0x00},
    { 0x0c, 0x00},
    { 0x0d, 0x00},
    { 0x0e, 0x00},
    { 0x0f, 0x00},

    { 0x15, 0x00},

    { 0x27, 0x80},
    { 0x2a, 0x00},
    { 0x2b, 0x03},
    { 0x2f, 0x00},

    { 0x30, 0x01},
    { 0x31, 0x0a},
    { 0x34, 0x20},
    { 0x3a, 0x00},
    { 0x3b, 0x00},
    { 0x3c, 0x00},
    { 0x122, 0x02},
    { 0x134, 0x24},
    { 0x222, 0x02},
    { 0x234, 0x24},
    { 0x422, 0x02},
    { 0x434, 0x24},
    { 0x522, 0x02},
    { 0x534, 0x24}
};
```

9 Appendix B - LMK04828B Configuration

```
static const DEVICE_DATA defaultData [NUM_REGISTERS] =
{
    { 0x0000, 0x90}, // Init

    { 0x0000, 0x10},
    { 0x0002, 0x00},
    { 0x0003, 0x00},
    { 0x0004, 0x00},
```

```
{ 0x0005, 0x00},
{ 0x0006, 0x00},

{ 0x000c, 0x00},
{ 0x000d, 0x00},

{ 0x0100, 0x1e}, // DCLK0 Divide by 30
{ 0x0101, 0x55},
{ 0x0103, 0x00},
{ 0x0104, 0x22},
{ 0x0105, 0x00},
{ 0x0106, 0xf2},
{ 0x0107, 0x66},
{ 0x0108, 0x1e}, // DCLK2 Divide by 30
{ 0x0109, 0x55},
{ 0x010b, 0x00},
{ 0x010c, 0x22},
{ 0x010d, 0x00},
{ 0x010e, 0xf2},
{ 0x010f, 0x13}, // place DCLK2 out in hsds mode

{ 0x0110, 0x1e}, // DCLK4 Divide by 30
{ 0x0111, 0x55},
{ 0x0113, 0x00},
{ 0x0114, 0x22},
{ 0x0115, 0x00},
{ 0x0116, 0xf2},
{ 0x0117, 0x11},
{ 0x0118, 0x18},
{ 0x0119, 0x55},
{ 0x011b, 0x00},
{ 0x011c, 0x22},
{ 0x011d, 0x00},
{ 0x011e, 0xfb},
{ 0x011f, 0x00},

{ 0x0120, 0x08},
{ 0x0121, 0x55},
{ 0x0123, 0x00},
{ 0x0124, 0x22},
{ 0x0125, 0x00},
{ 0x0126, 0xfb},
{ 0x0127, 0x00},
{ 0x0128, 0x08},
{ 0x0129, 0x55},
{ 0x012b, 0x00},
{ 0x012c, 0x22},
{ 0x012d, 0x00},
{ 0x012e, 0xfb},
{ 0x012f, 0x00},

{ 0x0130, 0x06},
{ 0x0131, 0x55},
{ 0x0133, 0x00},
{ 0x0134, 0x22},
```

```
{ 0x0135, 0x00},
{ 0x0136, 0xfb},
{ 0x0137, 0x00},
{ 0x0138, 0x20},
{ 0x0139, 0x02}, // pulser sysref
{ 0x013a, 0x09}, //13a(09) 13b(60) set for 1.25M sysref
{ 0x013b, 0x60}, //13a(09) 13b(60) set for 1.25M sysref
{ 0x013c, 0x00},
{ 0x013d, 0x08},
{ 0x013e, 0x03},
{ 0x013f, 0x00},

{ 0x0140, 0x03},
{ 0x0141, 0x00},
{ 0x0142, 0x00},
{ 0x0143, 0x51},
{ 0x0144, 0x83},
{ 0x0145, 0x7f},
{ 0x0146, 0x0f},
{ 0x0147, 0x3a},
{ 0x0148, 0x02},
{ 0x0149, 0x42},
{ 0x014a, 0x33},
{ 0x014b, 0x16},
{ 0x014c, 0x00},
{ 0x014d, 0x00},
{ 0x014e, 0xc0},
{ 0x014f, 0x7f},

{ 0x0150, 0x03},
{ 0x0151, 0x02},
{ 0x0152, 0x00},
{ 0x0153, 0x00},
{ 0x0154, 0x01},
{ 0x0155, 0x00},
{ 0x0156, 0x01},
{ 0x0157, 0x00},
{ 0x0158, 0x00},
{ 0x0159, 0x00},
{ 0x015a, 0x0a},
{ 0x015b, 0x1f},
{ 0x015c, 0x20},
{ 0x015d, 0x00},
{ 0x015e, 0x00},
{ 0x015f, 0x0b},

{ 0x0160, 0x00},
{ 0x0161, 0x01},
{ 0x0162, 0x44},
{ 0x0163, 0x00},
{ 0x0164, 0x00},
{ 0x0165, 0x0c},

{ 0x017c, 0x15}, // Program before PLL2 register
{ 0x017d, 0x33}, // to optimize VCO1 noise performance
```

```
    { 0x0166, 0x00}, // PLL2 registers
    { 0x0167, 0x00},
    { 0x0168, 0x0f},
    { 0x0169, 0x59},
    { 0x016a, 0x40},
    { 0x016b, 0x01},
    { 0x016c, 0x00},
    { 0x016d, 0x00},
    { 0x016e, 0x13},

    { 0x0173, 0x00},

    { 0x0182, 0x0},
    { 0x0183, 0x0},
    { 0x0184, 0x0},
    { 0x0185, 0x0},
    { 0x0188, 0x0},

    { 0x1ffd, 0x00},
    { 0x1ffe, 0x00},
    { 0x1fff, 0x53},

    { 0x0139, 0x00},
    { 0x0140, 0x00},
    { 0x0143, 0x91},
    { 0x013e, 0x03},
    { 0x0144, 0x00},
    { 0x0143, 0xb2},
    { 0x0143, 0x92},
    { 0x0144, 0xff},
    { 0x0143, 0x12},
    { 0x0139, 0x02},
    { 0x0143, 0x12},

};
```

10 Appendix B - HSMC Connector Pinout

Table 10-1 HSMC Connector (ASP-122952-01) Bank 1 Pin-out

Pin #	Bank	Signal	Pin #	Bank	Signal
1	1	No Connect	2	1	No Connect
3	1	No Connect	4	1	No Connect
5	1	No Connect	6	1	No Connect
7	1	No Connect	8	1	No Connect
9	1	No Connect	10	1	No Connect
11	1	No Connect	12	1	No Connect

13	1	No Connect	14	1	HSMC_DEVCLK_P
15	1	No Connect	16	1	HSMC_DEVCLK_N
17	1	No Connect	18	1	HSMC_GXB_RX3_P
19	1	No Connect	20	1	HSMC_GXB_RX3_N
21	1	No Connect	22	1	HSMC_GXB_RX2_P
23	1	No Connect	24	1	HSMC_GXB_RX2_N
25	1	No Connect	26	1	HSMC_GXB_RX1_P
27	1	No Connect	28	1	HSMC_GXB_RX1_N
29	1	No Connect	30	1	HSMC_GXB_RX0_P
31	1	No Connect	32	1	HSMC_GXB_RX0_N
33	1	No Connect	34	1	No Connect
35	1	No Connect	36	1	No Connect
37	1	No Connect	38	1	No Connect
39	1	No Connect	40	1	No Connect

Table 10-2 HSMC Connector (ASP-122952-01) Bank 2 Pin-out

Pin #	Bank	Signal	Pin #	Bank	Signal
41	2	No Connect	42	2	No Connect
43	2	No Connect	44	2	No Connect
45	2	3.3V	46	2	12V
47	2	LMK_MOSI	48	2	LMK_MISO
49	2	No Connect	50	2	No Connect
51	2	3.3V	52	2	12V
53	2	LMK_SCLK	54	2	ADS_MISO
55	2	No Connect	56	2	No Connect
57	2	3.3V	58	2	12V
59	2	LMK_SSN	60	2	HSMC_SYSREF_P
61	2	No Connect	62	2	HSMC_SYSREF_N
63	2	3.3V	64	2	12V
65	2	LMK_SYNC	66	2	OVR_CH0
67	2	No Connect	68	2	No Connect
69	2	3.3V	70	2	12V
71	2	ADS_MOSI	72	2	OVR_CH1

73	2	No Connect	74	2	No Connect
75	2	3.3V	76	2	12V
77	2	ADS_SCLK	78	2	OVR_CH2
79	2	No Connect	80	2	No Connect
81	2	3.3V	82	2	12V
83	2	ADS_SSN	84	2	OVR_CH3
85	2	No Connect	86	2	No Connect
87	2	3.3V	88	2	12V
89	2	ADS_PDN	90	2	No Connect
91	2	No Connect	92	2	No Connect
93	2	3.3V	94	2	12V
95	2	No Connect	96	2	HSMC_CLKIN1_P
97	2	No Connect	98	2	HSMC_CLKIN1_N
99	2	3.3V	100	2	12V

Table 10-3 HSMC Connector (ASP-122952-01) Bank 3 Pin-out

Pin #	Bank	Signal	Pin #	Bank	Signal
101	3	ADS_RESET	102	3	No Connect
103	3	No Connect	104	3	No Connect
105	3	3.3V	106	3	12V
107	3	ADS_SYNC_P	108	3	No Connect
109	3	ADS_SYNC_N	110	3	No Connect
111	3	3.3V	112	3	12V
113	3	EXT_TRIGGER	114	3	No Connect
115	3	No Connect	116	3	No Connect
117	3	3.3V	118	3	12V
119	3	No Connect	120	3	HSMC_SYSREF_P
121	3	No Connect	122	3	HSMC_SYSREF_N
123	3	3.3V	124	3	12V
125	3	No Connect	126	3	OVR_CH0
127	3	No Connect	128	3	No Connect
129	3	3.3V	130	3	12V
131	3	No Connect	132	3	No Connect

133	3	No Connect	134	3	No Connect
135	3	3.3V	136	3	12V
137	3	No Connect	138	3	No Connect
139	3	No Connect	140	3	No Connect
141	3	3.3V	142	3	12V
143	3	No Connect	144	3	No Connect
145	3	No Connect	146	3	No Connect
147	3	3.3V	148	3	12V
149	3	No Connect	150	3	No Connect
151	3	No Connect	152	3	No Connect
153	3	3.3V	154	3	12V
155	3	No Connect	156	3	HSMC_CLKIN2_P
157	3	No Connect	158	3	HSMC_CLKIN2_N
159	3	3.3V	160	3	PSNTn (GND)

Table 10-4 HSMC Connector (ASP-122952-01) GND Pin-out

Pin #	Bank	Signal	Pin #	Bank	Signal
161	1	GND	162	1	GND
163	1	GND	164	1	GND
165	2	GND	166	2	GND
167	2	GND	168	2	GND
169	3	GND	170	3	GND
171	3	GND	172	3	GND

11 Disclaimer

Information in this document concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. Customers are advised to obtain the latest version of device specifications before relying on any published information. Dallas Logic Corporation DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DATA FILES, DEVICES, OR TECHNOLOGY described in this document. Dallas Logic Corp. also does not assume liability for intellectual property infringement related in any manner to use of information, devices, or technology described herein or otherwise. Dallas Logic Corp. makes no warranty of merchantability or fitness for any purpose and does not assume liability for damages incurred to property due to the use of this product or implementation of information or procedures listed in this document. Use of information or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.