BEAGLE BONE BLE/WIFI CAPE

DEV-RF002 Datasheet

Version 1.3- May 2015

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Table of Revisions

Revision	Author	Date	Description
0.1	JT	03-20-2015	Initial
1.0	JT	05-27-2015	Pre-release
1.3	ET	05-31-2015	Minor edits before release

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1 Introduction

The DEV-RF002 is a combination Wi-Fi / BLE SMART communication module.

Below is a summary of the DEV-RF002 feature set:

- Texas instruments CC2650 SimpleLink™ Multi-standard wireless MCU (configured for BLE Smart).
  - Dedicated CJTAG programming header.
  - Dedicated Taiyo Yuden AH316M245001 chip antenna.
- Texas instruments CC3100 SimpleLink™ Wi-Fi® and Internet-of-Things solution for MCU applications.
  - Dedicated 8Mbit SPI configuration flash.
  - Dedicated Taiyo Yuden AH316M245001 chip antenna.
- Two 46 pin, 2.56mm pin headers (Beagle Bone Black compatible).
- RF switch footprint (future use).
- Beagle Bone Black configuration switch and serial flash footprint.

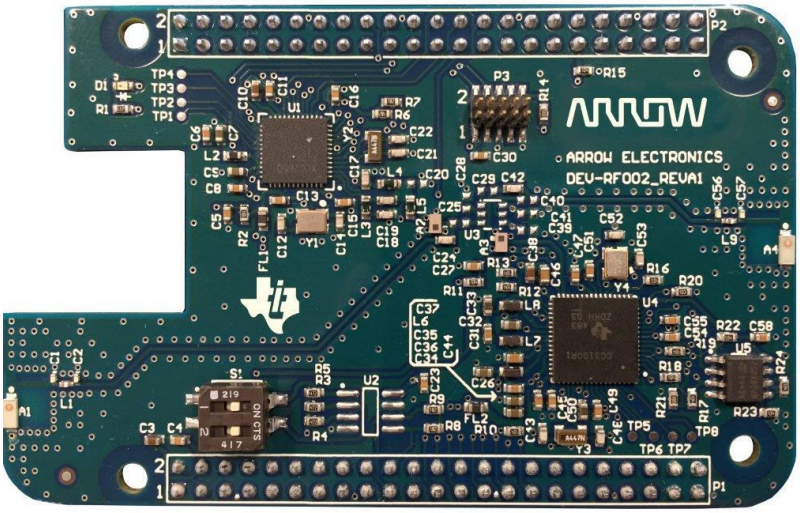

Figure 1-1 DEV-RF002 module

The RF002 is compatible with Arrow's MAX10 DECA board and the Beagle Bone Black via two 46 pin headers. The diagrams below provide the pin definitions for the P1 & P2 headers.

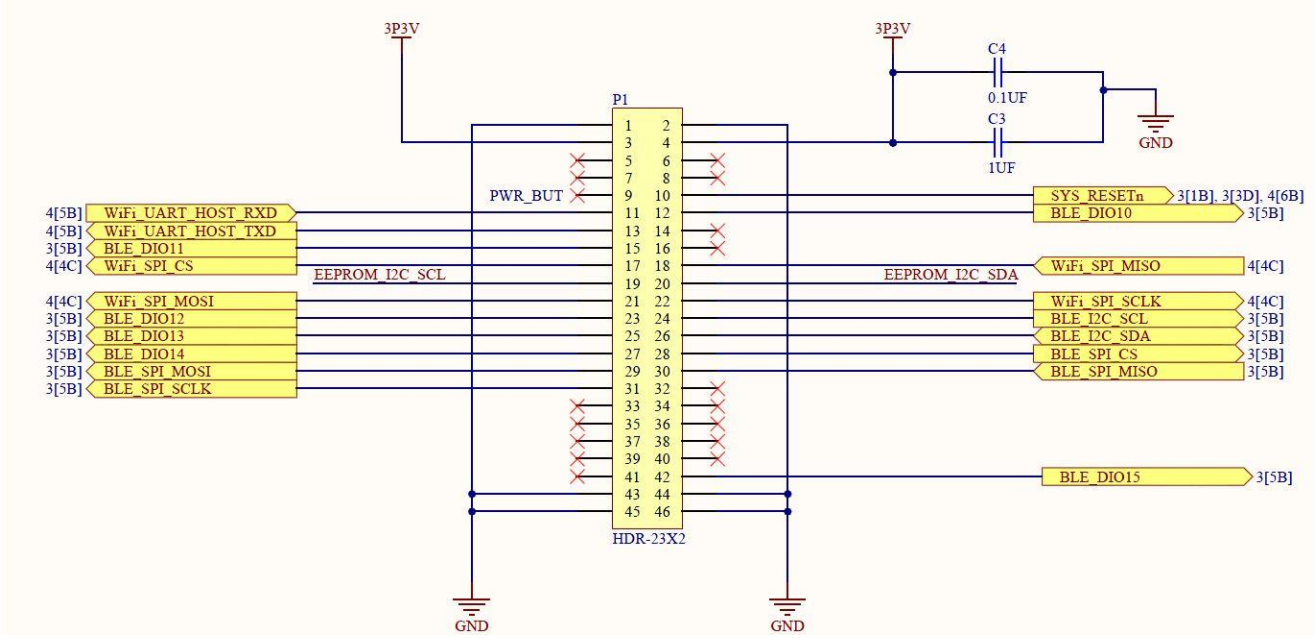

Figure 1-2 DEV_RF002 P1 pin header

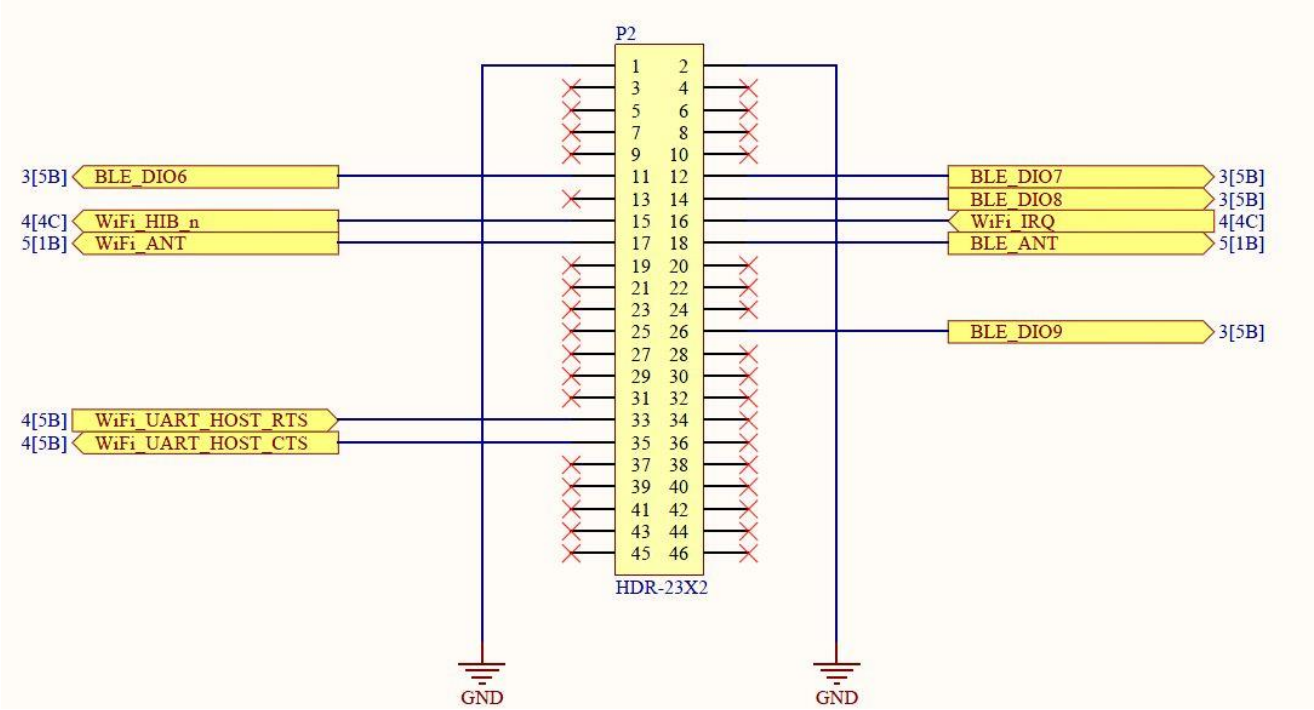

Figure 1-3 DEV-RF002 P2 pin header

1.1 DEV-RF002 Module Block Diagram

The diagram below provides an overview of the DEV-RF002's interconnect.

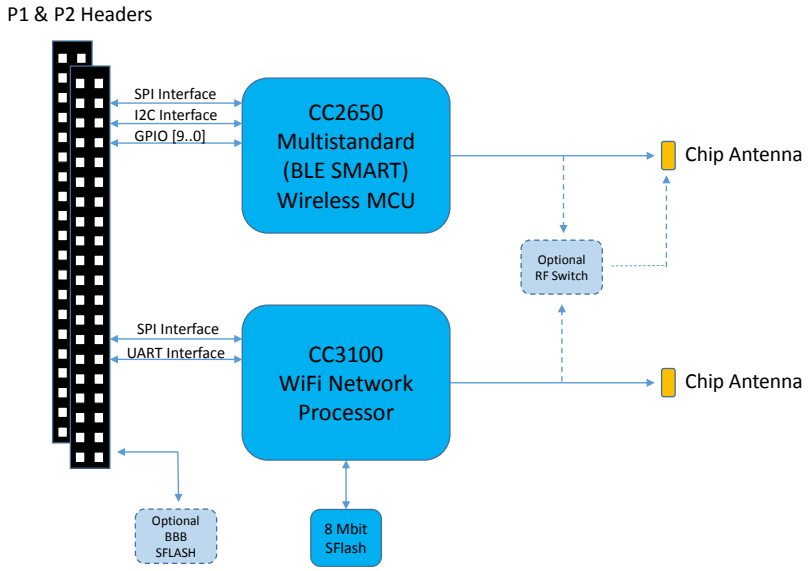

Figure 1-4 DEV-RF002 functional block diagram

2 RF Section

2.1 CC2650

The DEV-RF002 utilizes the Texas Instruments CC2650 to provide BLE connectivity. The CC2650 is a flexible wireless MCU that can be configured to provide various connectivity standards and includes numerous peripherals. The flexibility of the CC2650 allows it to be configured in many ways with respect to the RF interface, connectivity protocol, clocks, and power supplies. The default DEV-RF002 connectivity protocol is Bluetooth SMART. The protocol stack is stored internally in the CC2650 and is executed by a dedicated on-chip ARM Cortex®-M0 processor.

The two primary clocks for the CC2650 are provided by on board 24 MHz and 32.768 KHz crystals. While this configuration does not utilize any loading capacitors on the 24 MHz oscillator, the board design includes them to allow the use of different crystals as long as they have the same package.

The supply voltage configuration for the CC2650 utilizes the internal DC-DC converter. The 3.3VDC power rail from the P1 header is filtered and powers the three VDDS pins on the CC2650 along with the VDDS_DCDC pin. The output of the internal DC-DC converter is filtered and used to power the VDDR and VDDR_RF pins of the CC2650.

The CC2650 RF output pins (RF_P and RF_N) are combined into a single ended RF signal in a LC balun network before being routed to a Taiyo Yuden AH316M245001 chip antenna.

2.2 CC3100

The DEV-RF002 utilizes the Texas Instruments CC3100 to provide WiFi connectivity. The CC3100 is part of the SimpleLink Wi-Fi family that supports implementation of Internet connectivity. The CC3100 device integrates the required Wi-Fi and internet protocols.

The CC3100 includes an 802.11 b/g/n radio, baseband, and MAC with a crypto engine for secure internet connections with 256-bit encryption. The CC3100 device supports multiple operating modes including Station, Access Point, and Wi-Fi Direct. The device supports WPA2 personal and enterprise security and WPS 2.0 along with embedded TCP/IP and TLS/SSL stacks, HTTP server, and multiple Internet protocols.

The two primary clocks for the CC3100 on the DEV-RF002 are provided by on board 40 MHz and 32.768 KHz crystals.

The 3.3VDC power rail from the P1 header is filtered and powers the three internal DC-DC converters of the CC3100 (Analog, Digital, and PA) along with the VDD pins for the input I/O voltage rail and the onboard configuration flash.

The CC3100 UART and SPI interfaces are routed to the P1 and P2 headers.

Configuration data for the CC3100 is stored in an on board 8Mbit SPI flash. The flash storage is connected to the CC3100 FLASH_SPI pins.

The RF output pin (RF_BG) is routed to a Taiyo Yuden AH316M245001 chip antenna.

2.3 Antenna Configuration Options

The default configuration of the DEV-RF002 has the BLE and WiFi radios each connected to independent chip antennas. The antennas are physically located on opposite ends of the DEV-RF002 board to maximize the isolation between the antennas. This is the preferred configuration for the DEV-RF002 board.

The DEV-RF002 has been designed to allow the BLE and WiFi radios to share a common antenna. To utilize this functionality, several parts must be placed on the board that are not normally populated. These include 47 pF capacitors in C25, C28, C29, and C40 along with 0.1 uF capacitors in C39 and C41. In addition the RF switch MASW-007935 must be installed in U3. Finally, capacitors C24 and C42 must be removed from the board.

Once these changes are implemented the signals WiFi_ANT and BLE_ANT on the P2 header may be used to connect either the BLE or WiFi radio to the chip antenna located in reference designator A4.

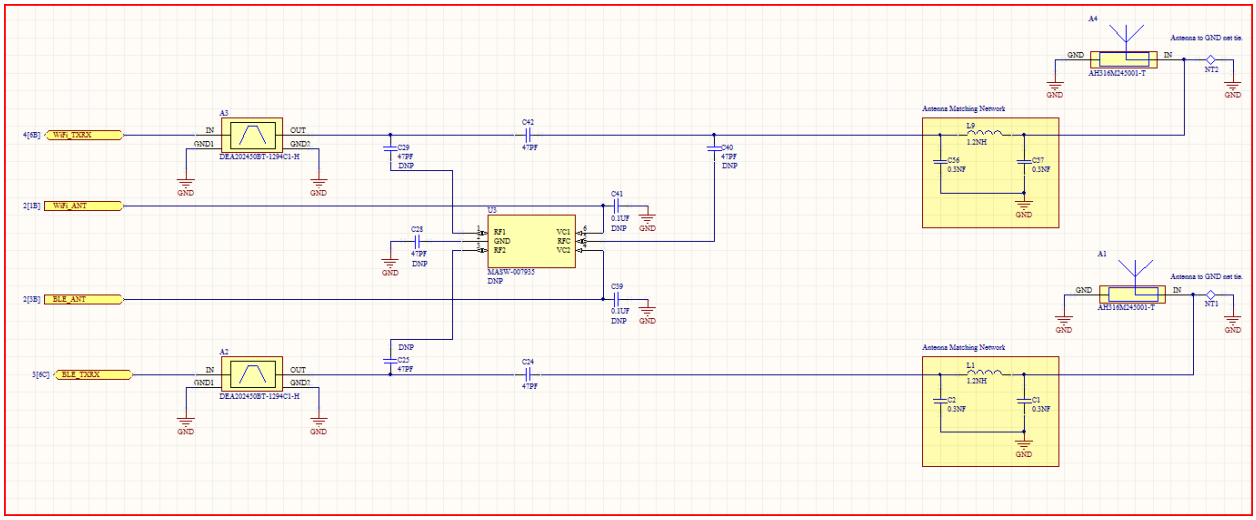

Figure 2-1 DEV-RF002 Antenna Selection Configuration

3 Digital Specifications

3.1 CC2650 Hardware

The DEV-RF002 supports several communication interfaces which are provided by the CC2650 device. Included are one 4 wire SPI interface and one I2C interface. These interfaces are provided as pin connections on the modules P1 and P2 headers. Ten additional GPIO are available on the CC2650. These IO can be configured as generic peripheral input / output pins or programmed as communication interfaces including SPI, I2C and UART.

3.1.1 CC2650 Pin Definitions

Table 3-1 CC2650 Pin Description

Pin Name	Description	Header & Pin Number
BLE_I2C_SCL	I2C clock pin	P1 (24)
BLE_I2C_SDA	I2C data pin	P1 (26)
BLE_SPI_CSN (CC2650 configured as Master)	Serial Peripheral Interface (SPI) chip select active low	P1 (28)
BLE_SPI_MISO (CC2650 configured as Master)	Serial Peripheral Interface (SPI) Master In Slave Out	P1 (30)
BLE_SPI_MOSI (CC2650 configured as Master)	Serial Peripheral Interface (SPI) Master Out Slave In	P1 (29)
BLE_SPI_SCLK (CC2650	Serial Peripheral Interface (SPI)	P1 (31)

configured as Master)	Clock	
BLE_DIO15	Interrupt (Sourced from CC2650)	P1 (42)
BLE_DIO6– BLE_DIO9	Spare IO	P2 (11, 12, 14, 26)
BLE_DIO10– BLE_DIO14	Spare IO	P1 (12, 15, 23, 25, 27)
BLE_ANT	CC2650 Antenna switch (Not Used)	P2 (18)

3.1.2 CC2650 programming interface

The CC2650 uses an IEEE 1149.7 compliant compact JTAG (cJTAG) programming interface. cJTAG is a 2 pin communication protocol that is a subset of the standard 4 pin JTAG interface. The cJTAG interface requires only the TCK and TMS signals. The diagram below shows the pinout of the CC2650's programming header.

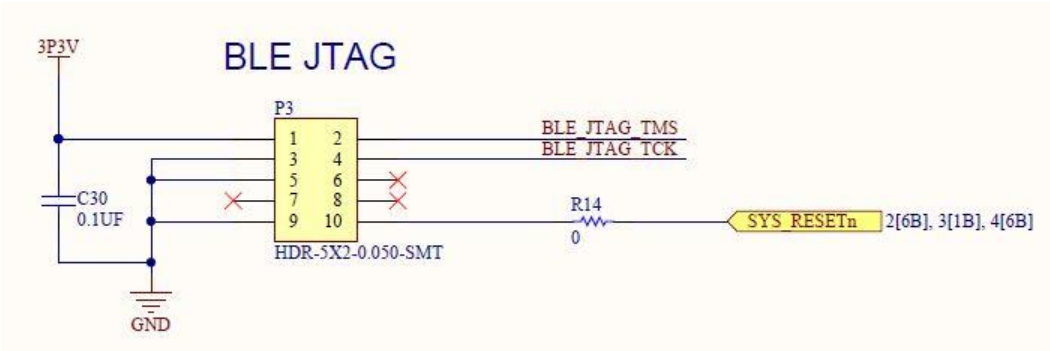

Figure 3-1 CC2650 cJTAG programming header

Physically, the header is a 10 pin (2x5), 1.27mm (.050") pitch, male header. The following programmer can be used to program the on board CC2650: http://www.ti.com/tool/cc-debugger

For additional details regarding programming the CC2650 please refer to the Texas Instruments CC2650 webpage: http://www.ti.com/product/CC2650/description

3.2 CC3100 Hardware

The DEV-RF002 supports two communication interfaces which are dedicated to the CC3100 device. These interfaces include one SPI interface and one UART interface. Both interfaces are provided as signals on connectors P1 and P2.

3.2.1 CC3100 Pin Definitions

Table 3-2 CC3100 pin description

Pin Name	Description	Header & Pin Number
WiFi_UART_HOST_RXD	CC3100 UART receive pin. TXD / RXD Crossover on module	P1 (11)
WiFi_UART_HOST_TXD	CC3100 UART transmit pin. TXD / RXD Crossover on module	P1 (13)
WiFi_UART_HOST_RTS	CC3100 UART request to send pin. RTS / CTS Crossover on module	P2 (33)
WiFi_UART_HOST_CTS	CC3100 UART clear to send pin. RTS / CTS Crossover on module	P2 (35)
WiFi_SPI_CSN (CC3100 configured as Slave)	Serial Peripheral Interface (SPI) chip select active low	P1 (17)
WiFi_SPI_MISO (CC3100 configured as Slave)	Serial Peripheral Interface (SPI) Master In Slave Out	P1 (18)
WiFi_SPI_MOSI (CC3100 configured as Slave)	Serial Peripheral Interface (SPI) Master Out Slave In	P1 (21)
WiFi_SPI_SCLK (CC3100 configured as Slave)	Serial Peripheral Interface (SPI) Clock	P1 (22)
WiFi_IRQ	Interrupt	P2 (16)
WiFi_HIB_N	CC3100 Hibernate, active low	P2 (5)
WiFi_ANT	CC3100 Antenna switch (Not Used)	P2 (17)

3.2.2 CC3100 Programming Interface

The CC3100 is configured by using an UART interface from either a PC or host controller. For example when connected with the DECA evaluation board, an Altera Nios II soft controller could be used to configure the CC3100. The CC3100 device maintains a proprietary file system on the attached 8Mbit serial flash. The file system stores the service pack file, system files, configuration files, certificate files, web page files, and user files.

For the current implementation, a UART pass through FPGA configuration was used to allow a PC based USB UART to connect directly to the CC3100. The Texas instrument's "Uniflash" tool was then used to program the serial flash. The Uniflash tool is available on a TI webpage located here: http://www.ti.com/tool/uniflash

An optional programming method was released by Texas Instruments after the completion of the current demo design. This method allows users to reprogram the CC3100's serial flash directly using the host MCU. A description of this technique can be found here:
http://processors.wiki.ti.com/index.php/CC31xx_Host_Programming_Application

3.3 Beagle Bone Black Configuration Interface

The DEV-Rf002 provides a footprint for a Beagle Bone Black (BBB) serial configuration device. Each cape must have its own EEPROM containing information that will allow the BBB to identify the board and to configure the expansion header pins as needed. The one exception is prototype boards. They may or may not have a EEPROM. This configuration device is not populated on the DEV-RF002.

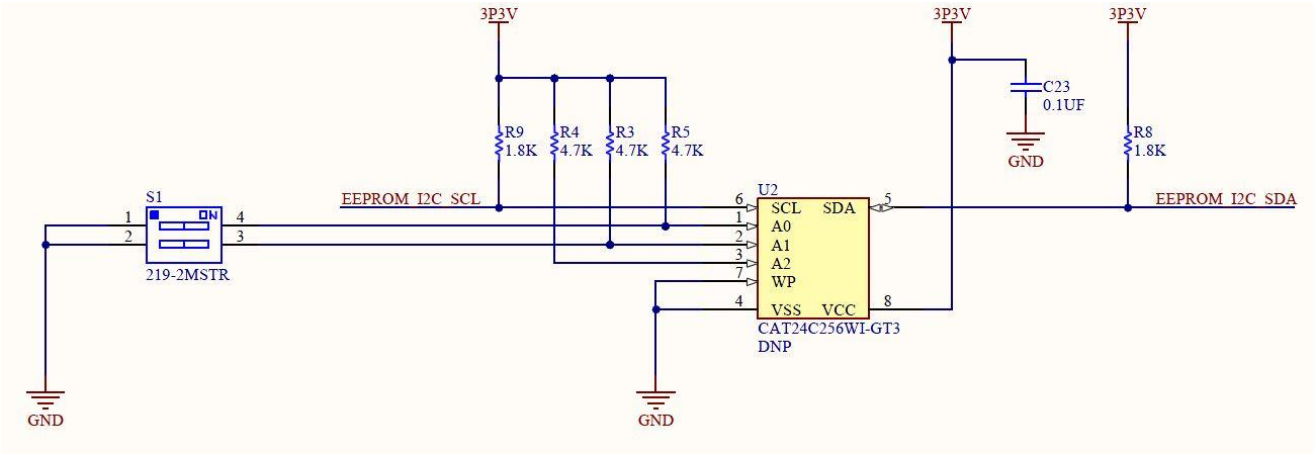

Figure 3-2 DEV-RF002 expansion EEprom circuit

3.4 MAX10 Software Support

The DEV-RF002 was designed to interface with Arrow's DECA evaluation board. The DECA features Altera's MAX10 FPGA and provides a number of onboard sensors. For the demo design, a Nios II soft controller was implemented to act as the host controller for both the CC3100 and CC2650. The Nios II was interfaced to each device using dedicated SPI interfaces.

3.4.1 Software Support

The NIOS II software on the DECA board is implemented as a single thread, non-OS system. The Nios II has a SPI driver for reading temperature and humidity data from the DECA board's HDC1000. The Nios II utilizes the MAX10s ADC to convert the accelerometer data from the LIS332AR.

The Nios II interfaces with CC2650 via SPI and signal BLE_DIO15 input, which is configured as an interrupt. Communication is initiated by the CC2650 by toggling BLE_DIO15. A signal transition on this pin will trigger a ISR to the Nios II. The ISR will begin shifting data to the CC2650. Following the assertion of the interrupt, the CC2650 can then clock data in from the Nios II host controller. The SPI interface on the Nios II controller is configured as an eight bit SPI slave. The CC2650 is configured to operate as the SPI master. This event occurs twelve times to complete the transmission of the temperature, humidity, and the XYZ accelerometer data. This cycle will occur every 500ms to coincide with the notification interval of 500ms. The notification interval is defined in the CC2650's BLE configuration.

As mentioned above, the CC3100 requires that the attached SPI flash be programmed prior to operation. The DEV-RF002 comes pre-configured with a demo design that is intended to be used with the DECA evaluation

board. The Nios II must utilize the SimpleLink device driver port to properly communicate with the CC3100. Communication with CC3100 is initiated on the Nios II by setting the WiFi_HIB_N line low. The CC3100 will synchronize with the Nios II by toggling the WiFi_IRQ signal. This will trigger the ISR written for the SimpleLink driver. The Nios II will drive WiFi_HIB_N line high to complete the response and allow the driver to complete the initialization process. The Nios II will proceed to configure the CC3100 device into an access point mode with DHCP and HTTP web server enabled. WLAN event handler is written to process connection and disconnection events. HTTP event handler is written to process POST/GET request by updating token values passed from the server. The same sensor data supplied to the CC2650 is transmitted to the CC3100 for display in a status webpage. In addition to the displaying the sensor data, the webpage offers users a method to control the LEDs located on the DECA evaluation bard.

3.5 Beagle Bone Black Board Support

The DEV-RF002 was designed to interface with the Beagle Bone Black. The module has been verified electrically to interface with the BBB.

3.5.1 Software Support

The Beagle Bone Black will require a port of the SimpleLink device driver in order to properly communicate with the CC3100. Additionally, a SPI device driver with ISR is required to interface with the CC2650.

4 Power Requirements

4.1 Voltage and Current Requirements

The DEV-RF002 requires that a 3.3V power supply be connected to pins 3 & 4 of the P1 pin header. Both the CC2650 and CC3100 devices have on chip voltage regulators that provide the necessary power regulation. Both devices can accept up to a 3.6V power supply.

Table 4-1 DEV-RF002 Voltage and Current by device

Device	Voltage Level	Current consumption active	Current consumption hibernate
CC3100	3.3V	TX (54 OFDM) **223mA**	**115uA** Sleep
		RX (54 OFDM) **53mA**	
CC2650	3.3V	TX (+5 dBm) **9.1mA**	**1uA**
		RX **5.9mA**	
Totals		TX **232.1mA**	**116uA**
		RX **58.9mA**	

5 Mechanical and Environmental

5.1 Mechanical

The DEV-RF002 PCB dimensions are based on the BeagleBone cape hardware specifications to allow mating with a BeagleBone compliant carrier.

The diagram below shows the mechanical dimensions of the DEV-RF002 BeagleBone cape. This diagram is re-printed here, for convenience, from the BeagleBone Black System Reference Manual Rev. C.1, page 114. This document can be referenced for more information on BeagleBone cape mechanical dimensions and other general technical information. The BeagleBone hardware support web page is located at:

http://beagleboard.org/Support/Hardware%20Support

The slot on the left side of the BeagleBone cape PCB outline is present to allow clearance for the Ethernet connector located on the BeagleBone host board. It also fixes the pin 1 orientation a cape can use to plug into a host carrier board (maintains proper pin 1 alignment).

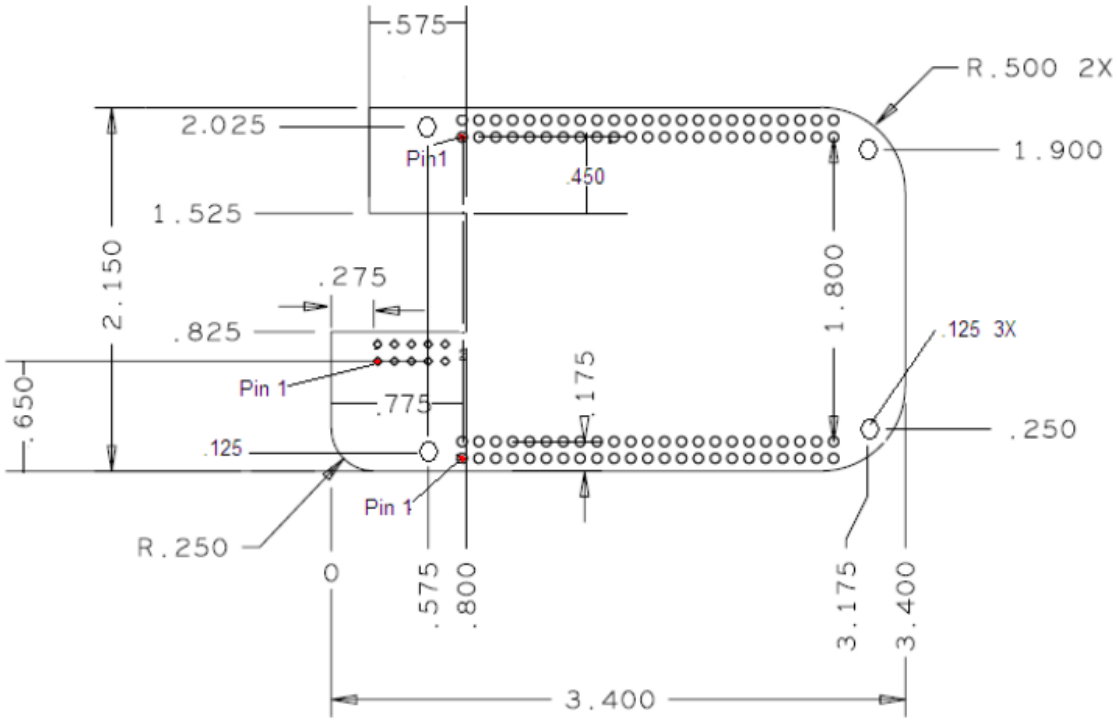

Figure 5-1 DEV-RF002 Module Mechanical Dimensions

The DEV-RF002 has components placed on the top side of the PCB only. This provides maximum dimensional clearance for components located on the host carrier board. The four tooling/mounting holes located at the four corners are 0.125in in diameter and are non-plated through holes (NPTH). The DEV-RF002 design uses four copper layers which include a power/ground plane pair, and a top and bottom routing layer pair.

The DEV-RF002 CAD image shown below indicates the locations of the components on the PCB. Note that most of the components are "low-profile" discrete and integrated circuit type devices. The P3 programming port and S1 dip switch are the only mechanical components which protrude well above the PCB surface (in addition to P1 and P2 BeagleBone cape connectors).

Two chip antennas (A1 and A4) are located to the far left and right sides of the PCB. These are the antennas for the BLE and WiFi devices respectively. They are located on the ends of the PCB to provide the required radiation properties and minimize interference between the two antenna devices. Also, the operation of the CC2650 and CC3100 devices provides for selection of different RF sub-channels based on channel noise parameters. Therefore, device operation is designed to minimize interference during simultaneous operation.

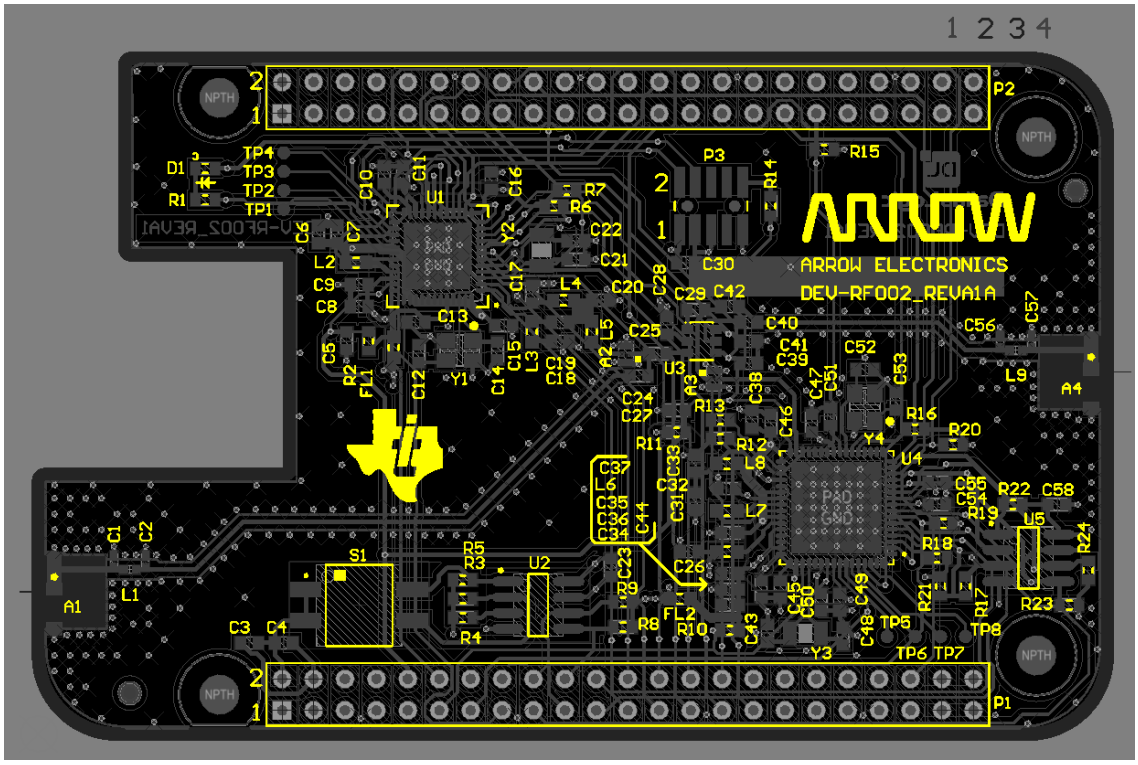

Figure 5-2 DEV-RF002 Module Device Reference Designators (CAD Image)

5.2 Environmental

The RF002 Wi-Fi BLE module is designed with commercial grade components, and is designed to operate over a temperature range of 0°C to 70°C.

6 References

1. BBONEBLK_SRM, BeagleBone Black System Reference Manual Rev C.1, May 2014.

2. SBAS669, CC2650 Datasheet, Texas Instruments, February 2015.

3. SWAS031C CC3100 Datasheet, Texas instruments, June 2013 – REVISED June 2014.

7 Disclaimer